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A Cost Efficient QCA Code Converters for Nano Communication Applications

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Abstract: Quantum-dot cellular automata (QCA) is an ingenious nano system prototype offers less dimensions with additional fast speeds related to CMOS design procedure. In this article an efficient QCA XOR gate and to explore the productiveness of the projected QCA XOR gate, various compound QCA diagrams like 4-bit, 8-bit, 16-bit and the 32-bit QCA layout of binary to gray (B2G) and gray to binary (G2B) code converters has been suggested. The suggested QCA layout is easy in design and effective in executing digital circuitry and conquers a fraction of the arena, as related to past designs. The suggested efficient XOR gate has only 09 cells and has 0.0180 μm2 arenas that is the least among all past designs. As per the performance execution parameter comparison, it is monitored that the suggested QCA architecture of 4-bit B2G and G2B achieve up to 41.26 and 45.61 percent enhancement creating them the most cost efficient QCA architectures. The suggested design is extended to n-bit code converters. These circuits are advisable for promoting the compound architectures. The functionality of suggested designs being inspected in QCADesigner simulation environment.

Keywords:QCA, XOR, B2G, G2B

1. Introduction and Overview

QCA could be non-transistor computation strategy that scrambles binary information via course of action of charges between quantum dots. Traditional CMOS has prevailed the fabricating industry for past decades, but presently we live in an exceedingly intellectual time with respect to innovations so our necessities for higher speed, decreased region, and low power could not be satisfied by conventional CMOS methodology. It is superior to move near-new options for IC Designing [1][2][3][4]. Very soon, QCA will be taken over CMOS due to its critical benefits. In this paper, first the designing of QCA XOR gate and application in designing of multiple bits code converters like B2G and G2B code converters and the suggested design is extended up to n-bit code converters by using the QCA designer tool and these proposed designs are improved as related to their best past designs regarding the area as well as latency. The proposed design is extended to n-bit code converters. These proposed designs are suitable for boosting the compound structures. QCA is the planned expansion of CMOS innovation since the straightforward impact of quantum concepts of the ever smaller transistor operation will not let more diminishment of simulation parameters in CMOS terminology. This technology can deliver exceptional device density, low power dissipation, and rapid switching.

A. Paper Alignment

The major improvements of this article are: a) Designing an ultra efficient QCA XOR gate (N9). b) Designing of cost efficient 4-bit, 8-bit, 16 bit and 32- bit B2G code converters. c) Designing of binary to gray code converter extended preferably n-bit (nB2G). d) Designing of cost efficient 4-bit, 8-bit, 16 bit and 32-bit G2B code converters. e) Designing of gray to binary code converter extended preferably n-bit (nG2B). f) The suggested designs are correlated to past layout in the parameters of quantum cell computation, arena, latency, and the quantum cost which asserts the recommended layout utilized less arena and superior quantum cost associated with the past layouts.

B. Paper Organization

The report is classified as Section-2 deals with the brief of QCA. The suggested QCA layout of XOR gate and code converters are explained in Section 3. Section-4 explained the simulation outcomes of the suggested layouts and compared to its past existing designs. At last, Section-5 summarized conclusion of the suggested exploration work.

2. An Outline of Quantum Dot Cellular Automata

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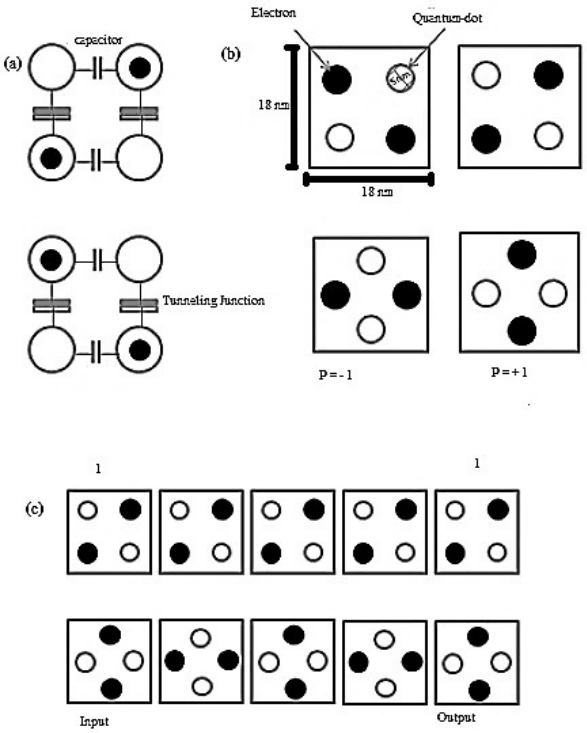

Figure 1. Cells in QCA (a) Functional Diagram (b) Cells Polarizations (c) QCA wire

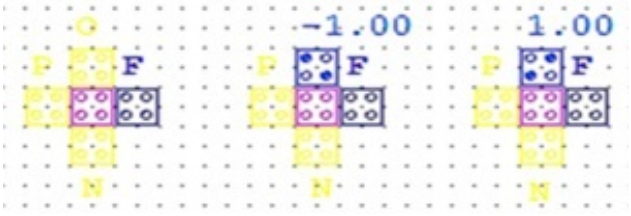

Figure 2. (a) Majority Gate (b) QCA AND Gate (c) QCA OR Gate: QCA Basic gates Layout

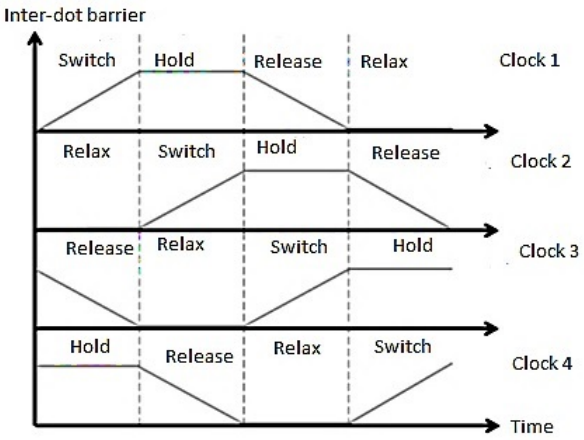

Figure 3. QCA Clocking: Four phase

QCA is an arrangement of action of quantum cells. The cell broadcast info electrostatically by neighboring cells. The cell is elaborated with a twin electrons in a cubicle [5][6][7]. QCA cells are arranged to create a QCA wire. The attraction and repulsion phenomenon takes place as the Columbic force among the electron and hole in the cell [8]

C. Majority Gate

Majority Gates is an arrangement of cells [9]. The output is

$$Y = XN + XZ + WZ \tag{1}$$

$$M(X, Z, W) = Y = (X * Z) + (W * Z) + (X * Z) \tag{2}$$

Where X, Z and W are 3 inputs and Y is the majority gate output, as presented in fig.2

D. QCA Clocking

The QCA clocking contains four stages:
1.Switch,
2.Control,
3. Release and
4. Relax as displayed in fig.3[10][11][12]

3. Proposed QCA XOR Gate Design

In this work we presented the QCA XOR Gate, which is further used for designing 4-bit QCA code converter circuitry. An efficient suggested QCA XOR (N9) is displayed in fig.4

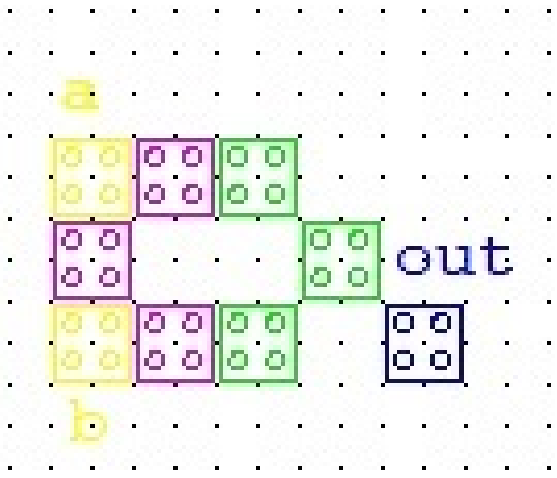

Figure 4. QCA Clocking: Four phase

In Niemier M.T.[13] designed QCA "XOR" containing 60 cells, 0.110 μm2 arena, and 1.5 clock cycle latency. The QCA layout conveyed a relevant cell count. To illuminate these issues, Hashemi S. et al. [14] suggested a new "XOR" gate having 51 cells only, 0.092 μm2 area and 2 clock cycle

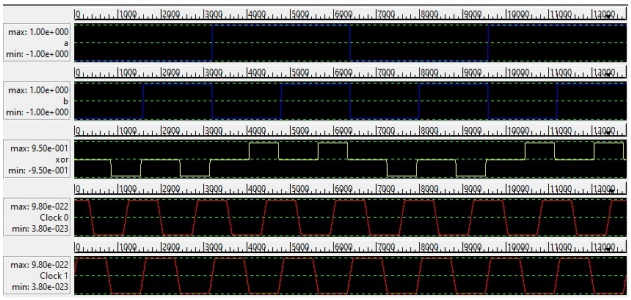

Figure 5. Simulation outcome waveform of suggested QCA XOR Gate (N9)

latency. Chabi A. M. et al.[15] which carry of 29 cells, 0.041 μm2 area having 0.25 clock cycle latency . Singh G. et al.[16], holding 28 cells, an area 0.035 μm2 and 0.75 clock cycle latency. Bahar A.N. et al.[17] suggested the cell number count is 12, area 0.021 μm2 and 0.05 latency.As per A. Roohi et al. [18] the XOR gate contains 14 number of cells, 0.034 μm2 area and 0.5 clock latency. As per Tripathi D. et. al[19] proposed 10 quantum cells XOR gate having 0.25 μm2 area.

4. QCA Based Proposed B2G Code Converters

E. Proposed QCA 4-bit B2G Code Converter

The circuitry that changes binary data to identical gray data, named as a B2G code converter[20][21]. Here, we planned 4- bit QCA B2G converter combined with planned QCA XOR gates. In suggested 4-bit QCA B2G code converter design coplanar crossovers technology is used.

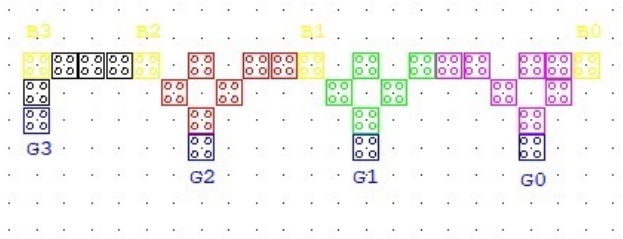

Figure 6. Suggested QCA 4-bit B2G code converter

F. Proposed QCA 8-bit B2G Code Converter

The planned 8-bit B2G code consists only 61 numbers of cells and an occupied arena of 0.11 μm2 and 0.75 clocking cycles latency. The projected QCA 8-bit B2G design consists of only efficient QCA XOR gate (N9) design.

G. Proposed QCA 16-bit B2G Code Converter

The planned 16-bit B2G converter layout is presented in fig.12 containing only 126 quantum cell count and having an area of 0.18 μm2.

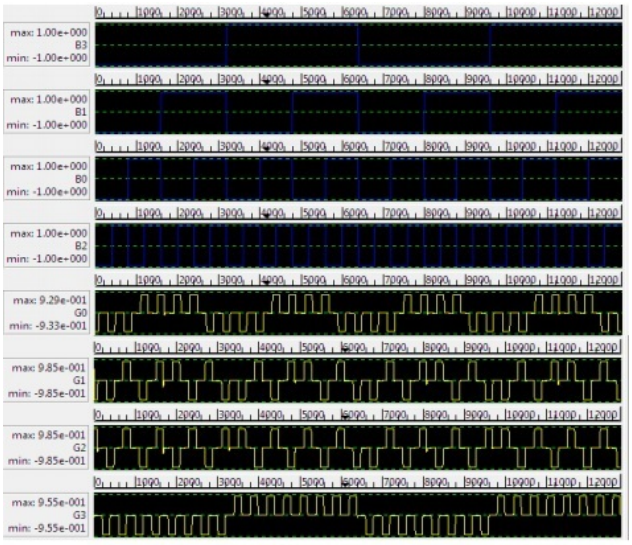

Figure 7. Simulation outcome waveform of the suggested 4-bit QCA B2G code converter

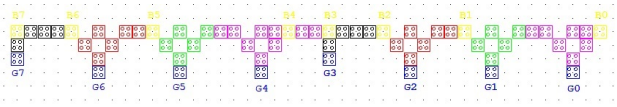

Figure 8. Suggested QCA 8-bit B2G converter

H. Proposed QCA 32-bit B2G Code Converter

The planned 32-bit B2G is explained in fig.13 containing only 252 quantum cells count and having an area of 0.53 μm2.

I. Proposed QCA n-bit B2G Code Converter

As per the comparative way, the suggested B2G converter could be amplified for n-bits. The proposed layout takes advantage of without a crossover and contains (n-1) QCA XOR (N9) gate. The number of cells for n-bit QCA layout will be 27+32(0.50n-1) occupied area of 0.3076+ 0.0235(0.50n-1) μm2 and latency is about 0.75n and clock cycles.

5. QCA Based Proposed G2B Code Converters

J. Proposed QCA 4-bit G2B Code Converter

The digital circuitry that converts gray code into its binary code is named G2B. The gray code is the unit code of distance codes, but not adapted to arithmetic functions[22][23][24]. Gray codes are extensively used in ADC and in error correction in digital communication also.

K. Proposed QCA 8-bit G2B Code Converter

The planned 8-bit G2B code contains only 52 quantum cells count and 0.09 μm2 an area and 0.75 clock cycles latency. The projected QCA 8-bit G2B design consists of only efficient QCA XOR gate (N9) design as displayed in fig. 11

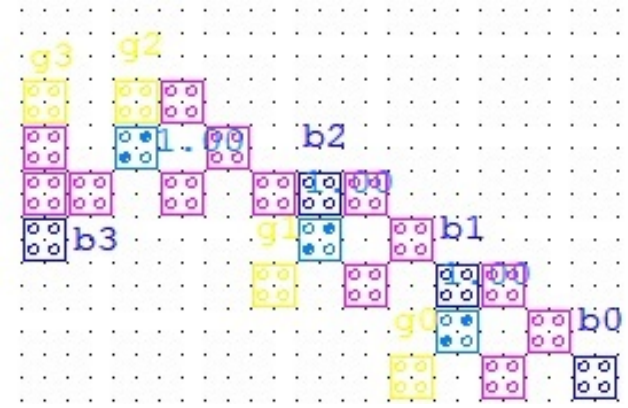

Figure 9. Suggested QCA 4-bit G2B converter

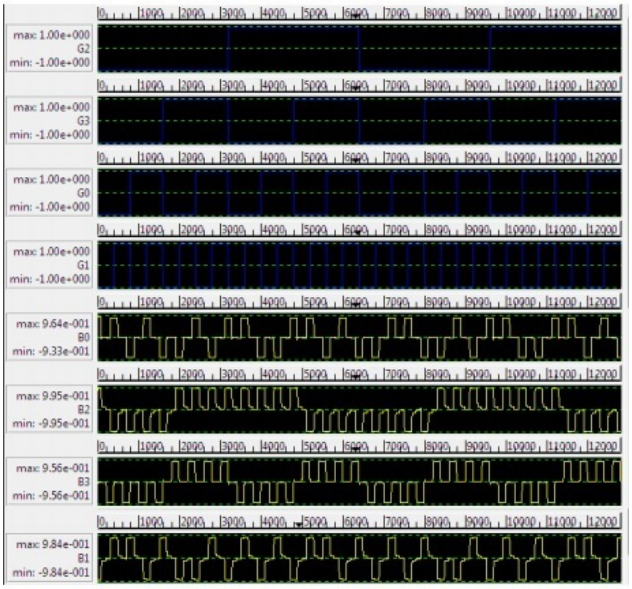

Figure 10. Suggested QCA 4-bit G2B converter

L. Proposed QCA 16-bit G2B Code Converter

The projected QCA 16-bit G2B code converter layout is presented in fig.14 containing only 106 quantum cells count and having an area of 0.36 μm2

M. Proposed QCA 32-bit G2B Code Converter

The planned QCA 32-bit G2B code converter layout is presented in fig. 15 containing only 212 quantum cells count and having an area of 0.93 μm2

N. Proposed QCA n-bit G2B Code Converter

As per the correlation, the suggested G2B may be amplified for n-bits. The proposed layout takes advantage of without a crossover and contains (n-1) QCA XOR (N9) gate. The number of cells for n-bit QCA layout would be 18+27 (0.50n-1) engrossed area of 0.2741+ 0.03810 (0.50n-1) μm2 and latency is of 0.75n clocking cycles.

6. Simulation Outcomes and Analysis

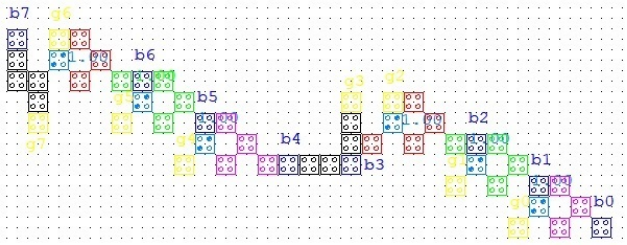

Figure 11. Suggested QCA 8-bit G2B converter

Figure 12. Suggested QCA 16-bit B2G Code Converter

QCADesigner tool is used for verification of the suggested layout. The parameters cell counts, arena and latency (clocking cycles) and quantum cost has been measured and matched that shows our proposed designs gained gained less QCA cells, more capable in the area, latency that compared to previous existing designs.Table–I represent the comparison of parameters of the QCA XOR gate and it shows the proposed design contains less quantum cells, arena and quantum cost as correlated to past designs.

The comparative result of B2G code converter is shown in Table-II, which explains the suggested design is better in terms of quantum cost,area and quantum cell as compared to previous designs.

The Table-III shows the correlation of QCA parameters like quantum cells, arena and quantum cost is compared which shows that the suggested design is best as related to its previous layouts.

The comparative quantum analysis shown that the suggested digital designs of QCA XOR gates, B2G and G2B code converters are cost efficient associated with its previous counterpart as mentioned in Fig.16, Fig.17and Fig.18.

7. Energy Dissipation of The Suggested QCA Designs

An add-on of QCADesigner is QCA Designer-E (QDE) of K. Walus. It executes the valuation of the energy dissipation of QCA architectures built on the study [25][26][27]. the QCA cell is in a depolarized state at the start of the clock cycle, energy must be gathered from the clock and surrounded by cells in order to achieve a polarisation state. In Table-IV presents energy dissipation of the suggested architectures presented at the given table the parameter like E bath total is the energy dissipation in each cycle, Sum bath is total energy dissipation, Ab, Ac is the average bath and average clock energy dissipation while simulation. The energy dissipation of suggested binary to gray (B2G) converter presented in table-IV and the energy dissipation of suggested gray to binary (G2B) converter presented in table-V.

TABLE I. PERFORMANCE RESEMBLANCE OF NUMEROUS QCA XOR DESIGN

QCA Design	QCA cell	Area (μm2)#	Latency(Clocking cycles)#	Quantum Cost(Area* Latency)
13	60	0.110	1.50	0.016
14	51	0.921	2.00	0.184
15	29	0.041	0.25	0.010
16	28	0.035	0.75	0.026
17	12	0.021	0.50	0.105
18	14	0.034	0.50	0.017
19	10	0.024	0.25	0.062
Suggested N9 XOR Gate	9	0.018	0.25	0.004

TABLE II. PERFORMANCE RESEMBLANCE TABLE OF NUMEROUS QCA B2G CODE CONVERTER DESIGN

QCA Designs	Bits	QCACells	Area (µm2)	Latency (Clock Cycle)	Quantum cost (Area *Latency)
[19]	4	33	0.08	0.75	0.045
[20]	4	97	0.18	0.25	0.045
[23]	4	93	0.16	0.75	0.121
[24]	4	99	0.09	0.75	0.067
[26]	4	33	0.14	0.50	0.066
	8	71	0.17	0.50	0.085
	16	147	0.28	0.50	0.140
	32	299	0.34	0.50	0.175
Suggested Designs	4	30	0.05	0.75	0.037
	8	61	0.11	0.75	0.080
	16	126	0.18	0.75	0.135
	32	252	0.53	1.00	0.530
	64	507	0.78	1.25	0.975
	n	27+32(0.50n-1)	0.3076+ 0.0235(0.50n-1)	0.75n	$0.30+0.0088n^2$-0.017n

TABLE III. PERFORMANCE RESEMBLANCE TABLE OF NUMEROUS QCA G2B CODE CONVERTER DESIGN

QCA Designs	Bits	QCA Cells	Area (μm^2)	Latency (Clock Cycle)	Quantum cost (Area *Latency)
[19]	4	25	0.05	1.00	0.050
[21]	4	69	0.17	0.75	0.045
[22]	4	99	0.15	0.75	0.112
[24]	4	115	0.15	1.50	0.225
[23]	4	76	0.07	2.25	0.157
[25]	4	121	0.16	2.5	0.410
[26]	4	63	0.06	1.00	0.127
	8	139	0.13	2.00	0.260
	16	291	0.27	4.00	1.080
	32	595	0.56	8.00	4.480
Suggested Designs	4	23	0.04	0.75	0.031
	8	52	0.09	0.75	0.067
	16	106	0.36	1.00	0.360
	32	216	0.92	1.50	1.381
	64	423	1.21	1.50	1.815
	n	18+27 (0.50n-1)	0.2741+ 0.03810 (0.50n-1)	0.75n	$0.0148n^2$-0285n+0.27

TABLE IV. Energy dissipation of the suggested QCA B2G code converter Designs

Suggested QCA Design	Bits	Sum_bath	Avg_bath	Sum_clk	Avg_clk
B2G Code Converter	4	2.02e-002 (Er: -1.74e-003)	1.84e-003 (Er: -1.58e-004)	5.99e-002	5.44e-003
	8	2.30e-002 (Er: -1.95e-003)	2.09e-003 (Er: -1.78e-004)	7.29e-002	6.63e-003
	16	4.25e-002 (Er: -1.63e-003)	5.07e-003 (Er: -2.16e-004)	8.54e-002	7.72e-003
	32	5.27-002 (Er: -2.91e-003)	6.23e-003 (Er: -3.12e-004)	7.24e-003	8.91e-003
	64	7.86-002 (Er: -3.85e-003)	8.23e-003 (Er: -2.24e-004)	8.16e-004	9.11e-004

TABLE V. Energy dissipation of the suggested QCA G2B code converter Designs

Suggested QCA Design	Bits	Sum_bath	Avg_bath	Sum_clk	Avg_clk
G2B Code Converter	4	3.35e-002 (Er: -3.62e-003)	3.04e-003 (Er: -3.29e-004)	2.85e-002	2.59e-003
	8	2.38e-002 (Er: -2.38e-003)	2.17e-003 (Er: -2.16e-004)	7.07e-002	6.42e-003
	16	4.70e-002 (Er: -4.67e-003)	4.28e-003 (Er: -4.25e-004)	1.56e-001	1.41e-002
	32	5.82e-002 **(Er: -6.53e-003)**	6.54e-003 (Er: -6.31e-004)	2.67e-002	2.61e-003
	64	7.61e-002 (Er: -4.45e-003)	8.56e-003 (Er: -5.41e-004)	4.87e-002	3.24e-003

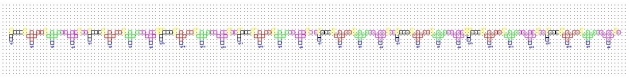

Figure 13. Suggested QCA 32-bit B2G Code Converter

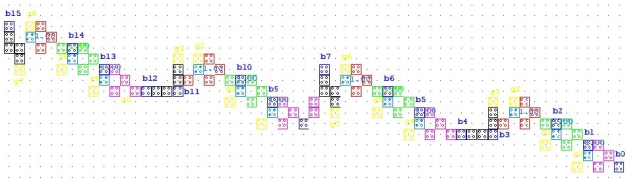

Figure 14. Suggested QCA 16-bit G2B code converter

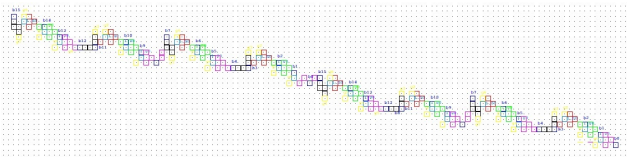

Figure 15. Suggested QCA 32-bit G2B code converter

8. Conclusion

Nano communication has been the main research area in the last ten years. This paper provided an optimal perspective to an XOR gate execution in QCA with less area, latency, and complexity related to its best existing counterpart for the verification and simulation QCA designer simulation environment. The suggested code converter topology like B2G and G2B code converter are explained. As per the performance execution parameter comparison, it is monitored that the suggested QCA architectures of 4-bit B2G and G2B gained up to 41.26 and 45.61 percent, 8-bit B2G and G2B 60 and 74 percent, 16- bit B2G and G2B 35 and 66 percent, 32-bit B2G and G2B 20 and 68 percent and in n-bit also respective enhancement in the terms of cost

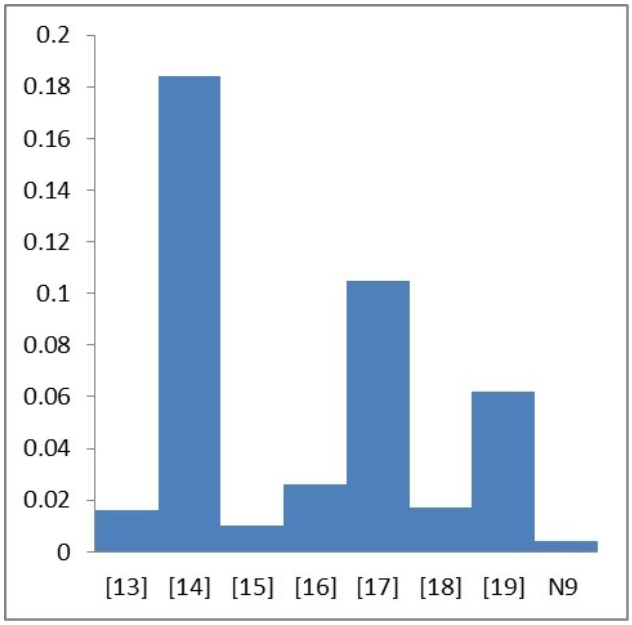

Figure 16. Fig.16. Quantum cost analysis of the Suggested QCA XOR Gate Designs

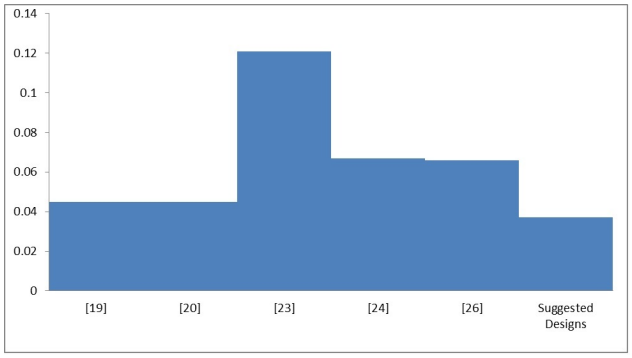

Figure 17. Quantum cost analysis of the Suggested QCA 4-bit B2G Code Converters Design

function of the circuitry in this manner creating them most cost efficient QCA architectures. The suggested designs have abundantly reduced the occupied area, that illustrates to be of an exceptional execution when considering huge and composite structures like ALU, processors, etc and further used to design any compound structures. In future the suggested circuitry will be used to create any multi layer, reversible and any error detection and correction circuits for nano communication applications. In this article, we optimized QCA cell counts, diminished the arena, quantum cost , and latency of suggested circuit designs associated to past layouts.

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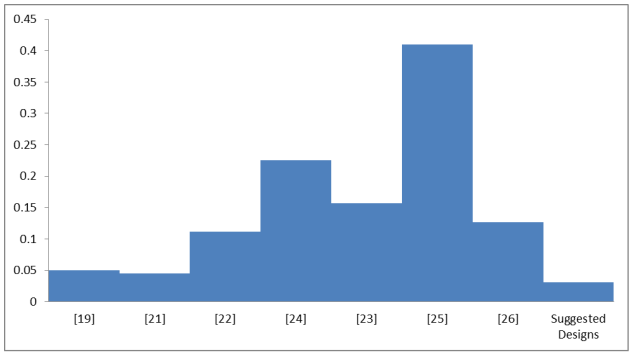

Figure 18. Quantum cost analysis of the Suggested QCA 4-bit G2B Code Converters Design

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