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Analysis on Digital Implementation of Sigma-Delta ADC with Passive Analog Components

HarshaVardhini Palagiri[1] , MadhaviLatha Makkena[2] , KrishnaReddyChantigari[3]

[1] *Associate Professor, Department of ECE, V.I.T.S, Deshmukhi, Hyderabad, A.P, India.*
pahv19@rediffmail.com
[2] *Professor, Department of ECE, J.N.T.U, Hyderabad, A.P, India.*
mlmakkena@yahoo.com
[3] *Director, NNRES group of institutions, Hyderabad, A.P, India.*
cvkreddy2@gmail.com

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Abstract: Sigma-Delta Analog to Digital Converter with digital implementation techniques is simulated. The differential pin based and inverter based architectures are discussed. Simulation of the proposed architecture with Virtex-4 FPGA I/Os is performed and analysis carried out using HSPICE to estimate the typical achievable clock speeds. The results demonstrate 200MHz clock speeds on LVPECL differential input pin for comparator action. Subsequently MATLAB simulation is carried out to simulate the digital blocks of SD-ADC. The results show promising direction of research for realizing SD-ADCs with only passive analog components outside the FPGA/ASIC.

Keywords: sigma-delta ADC, differential I/Os, all-digital-ADC, spartan-6 IBISmodel simulation, Select-IO technology, SFDR.

I. INTRODUCTION

Sigma-Delta (SD) analog to digital converters (ADCs) have several advantages over the nyquist rate type ADCs. The linearity over high dynamic range makes the SD ADCs an ideal choice for voice and precise instrumentation applications. The SD-ADC architecture is well established and analyzed [5, 6]. It is heavily based on digital processing and provides a high resolution, low noise output with very low analog implementation effort.

The technique of sigma delta ADC is in practice from several decades. The feature of digital dominated design of SD-ADC makes it different from other types of ADCs. As the technologies are evolving, new realization methodologies are emerging for realizing SD-ADC. The conventional approach of realizing an ADC as a separate ASIC and providing the interface to digital IC (either Microprocessor or FPGA) for providing mixed signal processing platform has following limitations.

- In spite of tremendous growth in EDA for VLSI, the analog VLSI synthesis is not automated. Hence the ADC kind of mixed signal design circuit remains as challenge and heavily depends on experience VLSI designers.
- The ADC chip occupies additional space on the board.
- With more number of components the reliability is less
- The interface between ADC and ASIC/FPGA requires special attention in terms of protocol and timing
- Most of the ADC chips require a considerable number of passive components outside resulting in increase of BOM, board real estate and cost.
- The number of ADC parameters that can be dynamically controlled from digital platform are limited and require separate interface (usually SPI or I2C).

The research towards all digital architectures is of interest to overcome some of these drawbacks. The work published in [13] uses Delay Locked loop (DLL) for realizing time based ADC. However this approach does not suit for FPGA based methodologies. The proposed approach aims to evolve ADC as an IP (intellectual property) realized in digital platform to overcome above described limitations at the expense of occupied slices (FPGA) or processing cycles (processor). The work is motivated by the upcoming mixed signal IP technologies

and new 7 series Xilinx FPGAs with Agile Mixed Signal (AMS) technology [12]. The 7 series Agile Mixed Signal (AMS) technology from Xilinx provides flexible general purpose analog interface. The work published in [10] explains this principle for ACTEL FPGAs, using FPGA differential pin as comparator. The paper shows above 75 dB SNR at 15 KHz sampling frequency, demonstrating its usage for sensor interfacing applications.

Even though the additional area occupancy or processor clock cycles penalty looks to be a drawback for this approach it is affordable due to below reasons.

- The FPGAs are dynamically configurable; hence multiple functionalities can be achieved with dynamic reconfiguration.
- The ADC samples will not be required in continuous fashion in most of the instrumentation and sensor networks applications. A set of samples at regular intervals of time are sufficient. High speed processors can spare few clock cycles for enabling ADC when ever required.

The work towards only digital active component based sigma-delta ADC is discussed in [1] for the power supply related parameters digitization. The paper describes the dynamic analysis for comparator which is realized by implementing the negative feedback around inverter. However this paper doesn't consider the threshold level variations of inverter gate which are possible in practical FPGA circuits. These variations become more crucial in low V_{dd} and high speed switches. The scheme given in [2] proposes a scheme for the architecture given in [1] to overcome the threshold level variations by adding passive components and using another differential output pin, which is working with same logic levels.

The papers [1] and [2] describe the inverter based comparator realization for implementing digital sigma delta ADC. The inverter based comparator is relatively slower mechanism resulting in overall reduced performance of the SD-ADC. As the comparator is realized with singled ended I/O inherently it will be slower in comparison with high speed differential I/Os which are exclusively designed for high data rates.

The work contributed by Altera group [3] uses FPGA I/O pads with low-voltage differential signaling (LVDS) as a comparator. The differential input pin is faster in comparison with single ended input pin when used as comparator. This is applicable for both Xilinx and Altera FPGAs and can be found in switching characteristics [4] of device data sheets. The work presented in [8, 9] describes the sigma delta ADC blocks including the decimation filters. The system generator based simulation results are presented. However the analog signal interfacing blocks are modeled with Simulink models and no practical implementation aspects are discussed. The paper given at [11] also describes only the FPGA prototyping of the sigma-delta ADC, but aimed for complete ASIC implementation.

In the context of passive analog and FPGA/ASIC based SD-ADC, only these [1] [2] [3] are the major works seen in literature. The continuously growing differential pin clock speeds of FPGA/ASIC IOs promises wide applications for this kind of ADCs in near future. The work presented here describes simulation of passive analog only SD-ADC with Xilinx Virtex-4 FPGAs with two high speed differential pins. The choice of Virtex-4 is due the availability of compatible simulation software and tools. However the methodologies presented here is technology independent and can be made applicable to 7-Series Xilinx FPGAs with latest version of H-SPICE simulation software. In case of 28 nm 7-series Xilinx FPGAs the achievable clock speeds will be even better.

II. COMPARATOR WITH DIFFERENTIAL FPGA I/O

The SD-ADC requires comparator with faster dynamic response and stable operating conditions to ensure guaranteed performance.

The FPGA differential pin is used as comparator here to carry following advantages over singled ended inverter based techniques.

- Tolerant to ground offsets, which could change based on the logic activity of the FPGA fabrics.
- Since the bias/reference supply is also on the same V_{dd} rail, the long term variations in the supply voltage effect the circuit in the similar manner as that of the variations in differential comparator I/O
- Resistance to EMI effects

A. Xilinx FPGA I/O Characterstics

The selected FPGA is from Virtex-4 family which supports several differential signal types. Among them the LVPECL is selected due to their fast switching speeds and sufficient input swing. The DC characteristics for LVPECL are given in the table I [4].

TABLE I. DC CHARACTERISTICS OF LVPECL STANDARD

Symbol	DC Parameter in volts	Min	Typ	max
VOH	Output high voltage	Vcc – 1.025	1.545	Vcc – 0.88
VOL	Output Low Voltage	Vcc – 1.81	0.795	Vcc – 1.62
VICM	Input Common-Mode voltage	0.6		2.2
VIDFF	Differential Input Voltage	0.100		1.5

From table I, it can be observed that the input signal allowed being with 0.7V maximum swing around the reference voltage. The reference voltage of 1.2V and peak to peak swing of input 0.6V is considered in the

present simulation. Xilinx provides simulation models for FPGA I/Os which are compatible with HSPICE simulator. In this work the Virtex-4 FPGA's LVPECL simulation model [7] is used for simulation.

The direct simulation of the LVPECL with H-SPICE simulator produces results as shown in Fig. 2. The input signal in1 and in2 are applied with 0.1V differential input pulse type sources which is minimum input differential signal required for this I/O standard.

It can be observed that after initial settling the LVDS_out signal produces output logic '1' when in1 in V_{ref} + 0.05V and in2 is V_{ref} – 0.05V. The input is switched at 400 MHz rate, i.e., the differential pins toggle for every 2.5 nsec. The same circuit with reduced input signal swing is simulated and observed that at same 200 MHz rate the output doesn't switch as per the input. The Fig. 3 shows the results for 400 µV differential (in1 and in2 swing between +/- 200 µV with respect to V_{ref}) input signal.

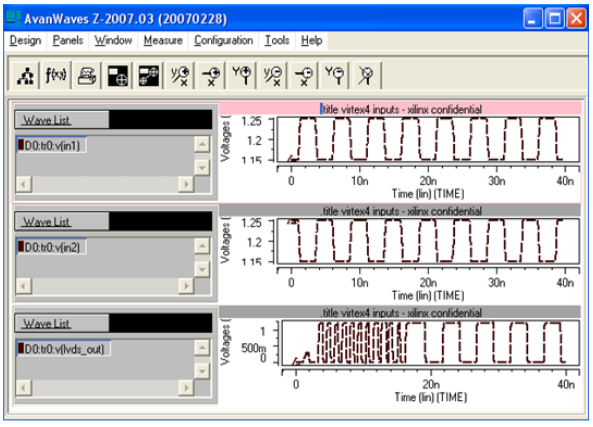

Fig. 2. Simulation of LVPECL pins with ideal input sources

The same circuit with reduced signal swing is simulated at 50 MHz switching rate and observed that the comparator action is achieved with correct results as in Fig. 4. This is in concurrence with theory of differential amplifier: As the input signal swing is less the differential amplifier takes higher settling time for output.

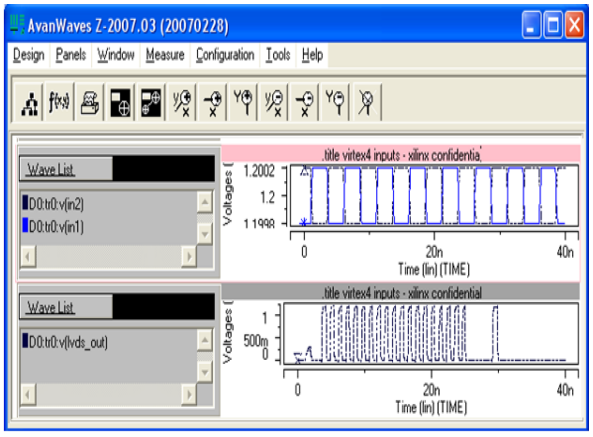

Fig. 3. Failure of differential pin at reduced signal swing and 200MHz

The simulation results prove that unconventional usage of differential input pin with reduced signal swing is possible for compromised clock speeds. To ensure that non-idealities are less in this nature of comparator realization, following factors must be considered at the design stage.

- As the output buffers within a given VCCO bank in FPGAs must share the same output drive source voltage. The output bank which we are using for driving single bit DAC must be load free.
- The V_{ref} must maintain minimum ripple and it is advisable to use external V_{ref} with stable value. Both the comparator and DAC must be from same bank and should utilize same V_{ref}
- Termination resistors are often required when using high-speed I/O standards for signaling.
- Slew rate can be set to fast
- Output drive strength can be kept maximum

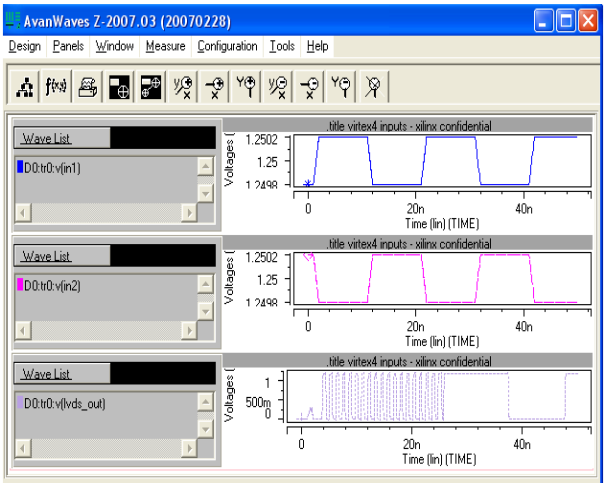

Fig. 4. Comparator action of differential pin at reduced swing and 50 MHz

Further simulation aspects of LVPECL differential pin in closed loop for SD-ADC are discussed in further sections.

III. SIGMA-DELTA ADC

The block diagram of SD-ADC simulated is given in Fig. 5. Two LVPECL pins of Virtex-4 FPGA are used for realizing the first order SD-ADC. The input signal is applied through coupling capacitor C_{in} and is to be expected to be at the offset of V_{ref} = 1.2V, with a swing of 0.6V.

B. H-SPICE Modeling of FPGA pins & analog passives

The increase in input signal increases V+ of comparator hence the comparator output turns logic '1'. Then the Capacitor C_{INT} sees V_{OH} as the final value to settle down. Hence the capacitor charges towards the final value V_{OH} with time constant $R_{INT}C_{INT}$. After some time the capacitor C_{INT} reaches higher than the voltage at

V+ then comparator output turns to logic'0'. How fast the integrator can track the input changes and provides sufficient swing at differential input decides the maximum rate at which the differential pin can be clocked. The integrator time constant must be decided considering the largest frequency of interest at input.

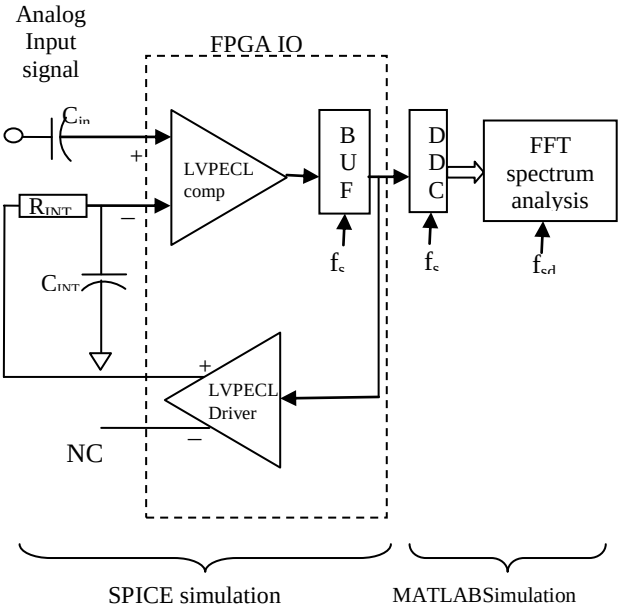

Fig. 5. Block diagram of SD-ADC used for simulation

The comparator output signal being "1" indicates that a positive excursion has occurred since the last sample, and a "0" indicates that a negative excursion has occurred since the last sample. If the input signal is near positive full-scale, it is clear that there will be more "1"s than "0"s in the bit stream. Likewise, for signals near negative full-scale, there will be more "0"s than "1"s in the bit stream. For signals near midscale, there will be approximately an equal number of "1"s and "0"s.

If the period at which the 1-bit DAC pin changes value is $T_{LVPECL\_CLK\_}$ then the pulse corresponding to one period duration starting at time T_o can be represented as below.

$$P_o = V\left[u\left(t-T_o\right)-u\left(t-T_o-T_{LVPECL\_CLK}\right)\right] \quad (1)$$

Where V is equal to $V_{OH,}$ when the digital value is logic '1' and $V_{OL,}$ when the digital value is logic '0'.

The first order RC network continuously gets the pulses from digital 1-bit DAC. The integrator action of RC network produces the integrated signal level at the input of the comparator. The input voltage to the first order RC network can be written as below.

$$V_i\left(n\right) = \sum_{k=0}^{n} \mathrm{P_i} \quad (2)$$

The v_i[n] is effective signal present at the input from 0 sec to i^{th} time period of $T_{LVPECL\_CLK.}$ To analyze the response of it the transient analysis must be done.

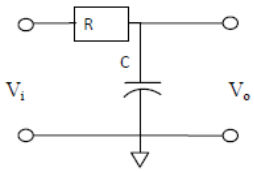

Fig. 6. RC circuit used as integrator

The RC circuit has following exponential response for step input with V volts.

$$V_o = V\left(1-e^{-t/RC}\right) \quad (3)$$

As the input to the RC circuit is sequence of pulses with V_L and V_H values, the voltage at the output of the RC integrator can be expressed as below.

$$V_o\left(n\right) = V_o\left(n-1\right)+\left(V_i\left(n\right)-V_o\left(n-1\right)\right)e^{-\frac{\text{Tclk\_LVDS}}{\tau}} \quad (4)$$

It is evident that under no noise conditions this voltage tracks the input signal in steps decided by the time constant and voltage difference between present voltage and end capacitor seen voltages (V_{OL} or V_{OH}).

Further simulation aspects using H-SPICE are given in section IV.

C. Modeling of complete SD-ADC

The h-SPICE simulation model is used to analyze the analog characteristics of the FPGA I/Os and further to estimate the typical clock frequencies at which the LVPECL buffer can run for selected time constant value. After deciding on this parameter the complete SD-ADC model is modeling in MATLAB including the analog and digital sections. The MATLAB simulation results are used to estimate the performance of whole SD-ADC. Consider the OSR of D is used at 1-bit ADC. The decimation low pass filter decimates by factor D. The resulting sampling rate can be given with below expression.

$$F_{sd} = \frac{F_{LVPECL\_CLK}}{D} \quad (5)$$

where F_{LVPECL_CLK} is the clock used in sampling the comparator output, is equivalent to f_s sampling rate of 1-bit ADC as shown in figure 5.

The purpose of the RC integrator in the feedback path is to maintain the average output of the integrator near to the input signal level. The density of "ones" at the modulator output is proportional to the input signal. For an increasing input the comparator generates a greater number of "ones," and vice versa for a decreasing input. By summing the error voltage, the integrator acts as a low pass filter to the input signal and a high pass filter to the quantization noise. Thus, most of the quantization noise is pushed into higher frequencies. It is to be noted that oversampling has changed not the total noise power, but its distribution. The decimation filter applied to the noise-shaped delta-sigma modulator, removes more noise than does simple oversampling.

TABLE II. SIMULATION PARAMETERS

Parameter	**Value**
Analog Section with R= 100Ω and C=1nF	
Input signal peak-to-peak	0.6 V
Input signal DC bias	1.2 V
Digital I/O	
F_{LVPECL_CLK}	200 MHz
V_L and V_H	0.9 V and 1.5 V
Decimation LPF : Sampling rate after decimation 500 KHz	
Filter order and BW	256 and 90% of output sample rate
Decimation factor	400

The simulation results for the MATLAB model with above parameters are discussed in section IV.

IV. SIMULATION RESULTS

As the usage of differential input LVPECL is in quite unconventional manner with low differential swings (even lower than values given in table I) the rated pin clock speeds as per data sheet cannot be considered here.

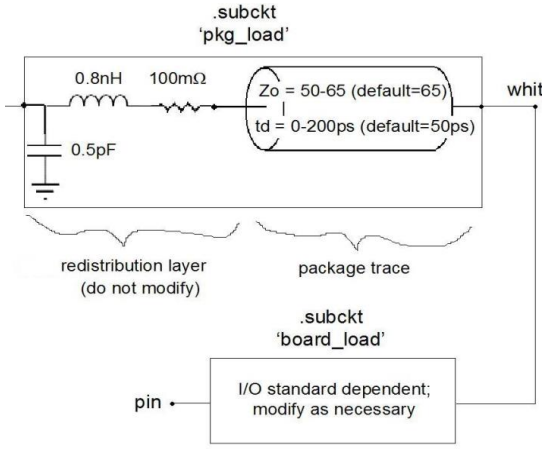

Fig. 7. Package parasitics of FPGA input/output buffer

The analog part in above described circuit is simulated in synopsis's H-SPICE tool. The FPGA pad and internal circuitry is modeled in Xilinx provided Virtex-4 models and the package parasitic model provided by Xilinx are added in netlist for simulation. The Fig. 7 shows the parasitic models used for I/Os [4]. The h-spice simulation results for circuit described in fig.5 are shown in fig.8.

From the simulation results it can be observed that capacitor voltage tracks the input signal. It is to be noted that the inverted logic exhibited at lvds_out signal is shown in simulation results. Hence under the positive excursion of input signal the pulse is low for more time and high for small time and vice versa. The inversion of this signal is used for digital processing in subsequent changes hence the final ADC samples will be computed correctly.

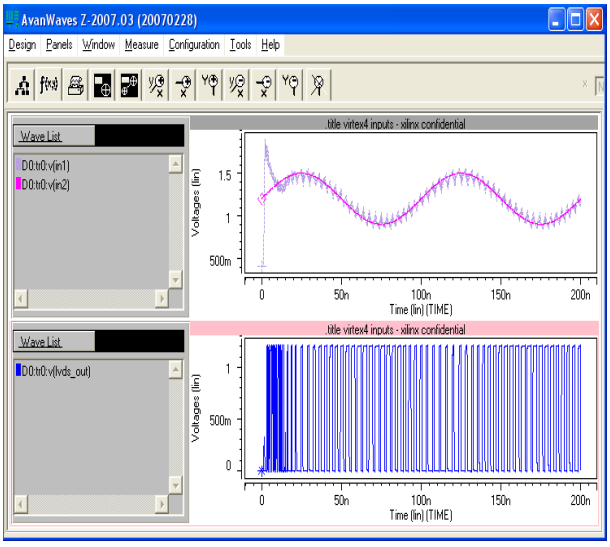

Fig. 8. Comparator output of SD-ADC

Further to the H-SPICE simulation complete analog and digital section of SD-ADC is simulated in MATLAB and following results are obtained. The Fig. 9 shows the capacitor voltage tracking at peaks of input signal and at the zero crossing. The Fig. 10 shows the FFT analysis of DDC output for single tone input signal. The Fig. 11 shows the 1024 point FFT analysis of DDC output for two tone input signal. Note that 4-term Blackman-Harris window function is used on DDC output before computing the FFT

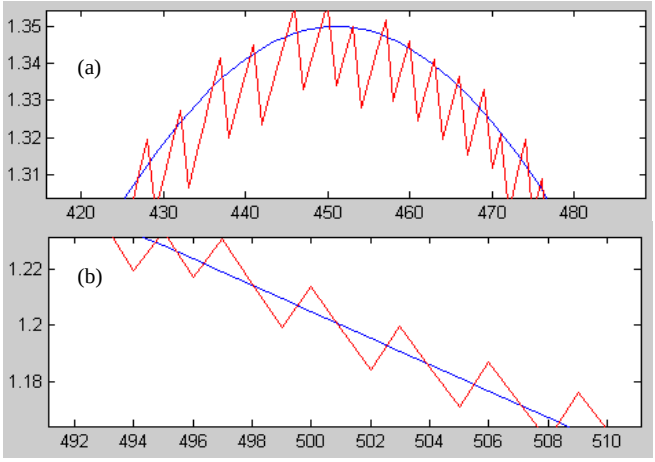

Fig. 9. Capacitor voltage tracking the input signal
(a) at positive peak (b) at zero crossing

In addition to the parameters given in table II the following parameters considered for generating test input signals.

Tone-1 input signal frequency fo=100e3

Tone 2 input signal frequency fo2=200e3

As the input signal is real, the spectrum is symmetric around bin 512. Hence two peaks are noticed in single tone case and similarly 4 peaks in two tone case.

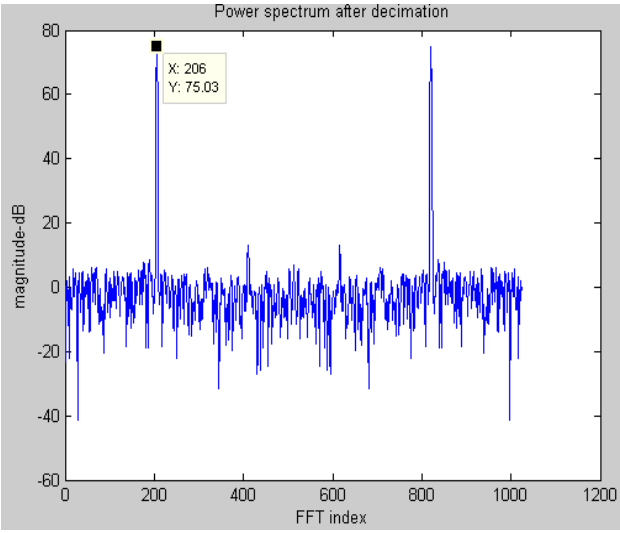

Fig. 10. FFT of single tone input signal

Linearity is very essential property for ADCs. The linearity ensures that no inter modulation (IMD) products are introduced when multiple single tone signals are applied. In practical usage of ADC the input signal can be viewed as multiple single tone signals. In ADCs, linearity is typically specified as SFDR. IMD is generally caused by modulation, and it can occur when an ADC samples a signal composed of two (or multiple) sine-wave signals. IMD spectral components can occur at both the sum (f_{IMF_SUM}) and the difference (f_{IMF_DIFF}) frequencies for all possible integer multiples of the fundamental (input

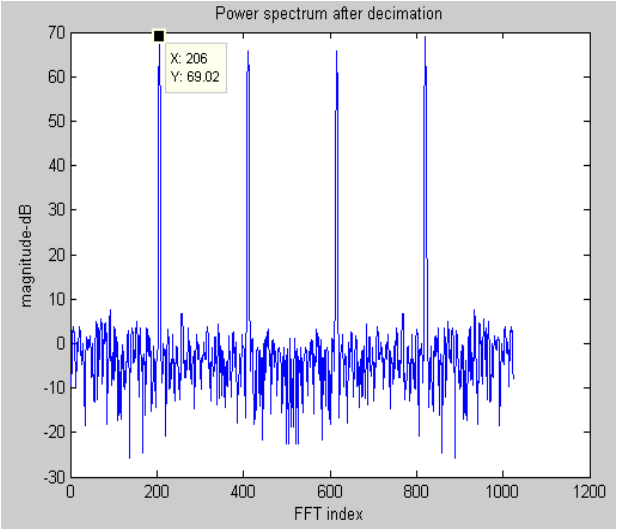

Fig. 11. FFT for two tone input signal

In the present simulation for the two-tone IMD test, the input test frequencies f_{IN1} and f_{IN2} are set to 100 KHz and 200 KHz values. The IMD amplitudes for a two-tone input signal are found at the specified sum and difference frequencies:

$$f_{IMF\_SUM} = \left|m \times f_{IN1} + n \times f_{IN2}\right| \text{ and } \left|m \times f_{IN1} - n \times f_{IN2}\right| \quad (6)$$

Where m and n are positive integers. The condition that m and n are greater than zero creates the 2nd-order ($f_{IN1} + f_{IN2}$ and $f_{IN1} - f_{IN2}$) and 3rd-order ($2f_{IN1} + f_{IN2}$, $2f_{IN1} - f_{IN2}$, $f_{IN1} + 2f_{IN2}$, and $f_{IN1} - 2f_{IN2}$, $3f_{IN1}$ and $3f_{IN2}$) intermodulation products.

The simulation results show that no intermodulation products are observed and the ADC has linear characteristics. Observing the highest spur at 10 dB, for the simulated circuit the single tone dynamic range observed is 65 dB. However as the peak input signal swing for both the input signals is set to half of the full scale value the two tone SFDR is 6 dB less than single tone SFDR.

V. CONCLUSION

Architecture for sigma delta ADC, which is possible to realize with discrete analog components and high speed LVPECL FPGA I/Os is presented. The architecture is aimed at evolving custom ADC design framework as an IP without separate VLSI design flow for ADC design. A single pole RC integrator is used to track the input analog signal and apply to the comparator configured from differential input signal. The single bit DAC is realized from another differential I/O of same logic type and set with same V_{ref}.

H-SPICE simulator is used to simulate the analog part and differential I/Os of the circuit. Xilinx provided Virtex-4's I/O pad and package SPICE models are used for this simulation. From these simulations it is concluded that LVPECL differential input pin working as comparator of Virtex-4 FPGA can be sampled at 200 MHz to give 1-bit ADC action.

Further to H-SPICE, MATLAB simulation is carried out with same analog component values. An OSR of 400 along with 200 MHz of 1-bit ADC sampling provides an effective SD-ADC sample rate of 500 KHz.

Single tone and two tone SFDR are computed and the circuit provides SFDR about 65 dB. The circuit performance can be further increased by increasing the OSR and using latest technology I/Os. Further improvement in analog circuit design by realizing the digital logic in FPGA is under investigation.

REFERENCES

[1] Jacomet, M., Goethe, J., Zbinden, V., and Narvaez, C., "On the dynamic behavior of a novel digital-only sigma–delta A/D converter". Proc. symp. Integrated Circuits and System Design, Pernambuco, Brazil, 2004, pp. 222–227

[2] J.I.Artigas, I.Urriza, D.Navarro, L.A.Barragan and J.Acero, "Comparator-less digital implementation of AC-coupled SD A/D converters" ELECTRONICS LETTERS 21st May 2009 Vol.45 No.11.

[3] Fabio Sousa, Volker Mauer, Neimar Duarte, Ricardo P. Jasinski and Volnei A. Pedroni, "Taking advantage of LVDS input buffers to implement sigma-delta A/D converters in FPGAs" Proc. Int. Symp. Circuits and Systems, Vancouver, BC, Canada, 2004, Vol.1, pp.1088–1091

[4] DC and switching characteristics of Virtex-4 FPGA device, http://www.xilinx.com/support/documentation/data_sheets/ds302.pdf

[5] M. Rebeschini et al, "A High-Resolution CMOS Sigma-Delta A/D Converter with 320 kHz Output Rate", Proc. ISCAS, pp. 246-249, 1989.

[6] R. Koch et al, "A 12-bit Sigma-Delta Analog-to-Digital Converter with a 15 MHz Clock Rate", IEEE J. of Solid-State Circuits, Vol. SC-21, No. 6, pp. 1003-1010, Dec. 1986.

[7] SPICE simulation models from Xilinx website. http://www.xilinx.com/support/download/index.htm

[8] Subir Kr. Maity and Himadri Sekhar Das, " FPGA Based Hardware Efficient Digital Decimation Filter for Σ-Δ ADC", International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, Volume-1, Issue-6, January 2012

[9] P. A. Uchagaonkar, S. A. Shinde, V.V. Patil and R.K. Kamat "FPGA based sigma –Delta analogue to digital converter design", International Journal of Electronics and Computer Science Engineering, ISSN-2277-1956/V1N2-508-513, Volume 1, 2012

[10] White paper "Stellamar Introduces All Digital, Fully Synthesizable Analog-to-Digital Converters for Microsemi FPGAs", Microsemi(Actel) June 2011.

[11] S. Kaur1 and P. S. Jassal, "Field Programmable Gate Array Implementation of 14 bit Sigma-Delta Analog to Digital Converter", International Journal of Emerging Trends & Technology in Computer Science (IJETTCS), ISSN 2278-6856, Volume 1, Issue 2, July – August 2012.

[12] A. Collins and R. Bielby, "Xilinx Agile Mixed Signal Solutions", Xilinx White paper, March 2012.

[13] Y. Lin and M. Ismail "Time-based all-digital sigma–delta modulators for nanometer low voltage CMOS data converters", Analog Integr Circ Sig Process 73:801–808, Springer 2012.