



# Adaptation of Feed-Forward Equalizer Settings: A Frequency Domain Analysis Approach

Ahmed M. Zaki<sup>1</sup>

<sup>1</sup>Department of Computer and Systems Engineering, Ain Shams University, Cairo, Egypt

Received 3 Jul. 2019, Revised 13 Sep. 2019, Accepted 20 Oct. 2019, Published 1 Nov. 2019

**Abstract:** Characteristics of the channel has a major effect on the signal integrity. The channel distortion is increased with high-rate data transmission. Feed-Forward Equalizer (FFE) at transmitter side is one of the methods that can be used to compensate the effect of the channel. PCIe-Gen3, 4, and 5 standards specify some constraints on the FFE settings and assign some preset values that can be used based on the effect of FFE on time-domain. In this paper, detailed analysis for the FFE in frequency domain is presented. New preset values are recommended to achieve enhancement on the behavior over different channels. Short and long channel models are created based on the PCIe standard specifications to check the suggested preset values with worst channels. Continuous-Time Linear Equalizer (CTLE) also is modeled to check the effect of FFE with different CTLE boost values. The eye-measurements based on the new preset values is enhanced by 10% with respect to the default preset values in PCIe specifications for short and long channel. Mapping the preset value in the frequency domain helps fine tuning process for FFE settings by facilitating more guidance to get the best FFE settings.

**Keywords:** Adaptation, Channel equalization, Feed-Forward Equalizer (FFE), Frequency domain analysis, Intersymbol interference (ISI), Signal integrity

## 1. INTRODUCTION

Serial data transmission is used in many applications. Characteristics of the channel affect signal integrity over channel. Signal attenuation is increased with high-rate data transmission, especially over long channels. Different attenuation on several frequency components distorts transmitted data waveform. Several techniques are used to fix channel distortion. The basic idea of equalization is to make equal attenuation at full signal frequency range up to Nyquist rate. For example, if the channel suffers attenuation on frequencies  $f_0$ ,  $f_1$ , and  $f_2$  by  $\alpha_0$ ,  $\alpha_1$ , and  $\alpha_2$  respectively, the equalizer has to increase the gain at  $f_0$ ,  $f_1$ , and  $f_2$  by  $\alpha_0^{-1}$ ,  $\alpha_1^{-1}$ , and  $\alpha_2^{-1}$  respectively. Equalization filters may be used at transmitter or receiver sides or at both of them to compensate the channel effect.

## 2. BACKGROUND

Several techniques can be used to compensate the channel effect on serial links. Continuous Time Linear Equalization (CTLE) [1]–[3], Feed-Forward-Equalizer (FFE) [4], [5], and Decision Feedback Equalizer (DFE) [6], [7]. FFE is used to increase the amplitude of the high-frequency components at the transmitter. CTLE is used to attenuate the low frequency components with respect to high-frequency at receiver sides. DFE is used at the receiver side to adjust the threshold of the slicers or add an offset to received signals based on previously received bits to eliminate the InterSymbol Interference

(ISI). Most adaption occurs at receiver side based on the signal integrity that is measured by the eye opening and indicated by Figure Of Merit (FOM). FFE is tuned at the transmitter side based on the FOM that is calculated at receiver side and retransmitted back to the transmitter side through back channel. Another technique is used to adapt the FFE based on an increment (INC) or a decrement (DEC) decision that it made at receiver side.

### A. Behavior of CTLE on PCIe-Gen3 (8.0 GT/s)

Equation (1) shows the transfer function of CTLE. By adjusting the transfer function parameters  $\omega_{p1}$ ,  $\omega_{p2}$ , and  $A_{DC}$  the gain can be adjusted over the frequency range to compensate the channel effect. where  $\omega_{p1}$  and  $\omega_{p2}$  are the first and second poles prospectively and  $A_{DC}$  is the DC-gain.

$$H(s) = \omega_{p2} \times \frac{s + \omega_{p1} \times A_{DC}}{(s + \omega_{p1})(s + \omega_{p2})} \quad (1)$$

PCIe-Gen3 specifications [8] sets appropriate values for  $\omega_{p1} = 2\pi \times 2GHz$ , and  $\omega_{p2} = 2\pi \times 8GHz$  to adjust the gain at Nyquist frequency 4 GHz for PCIe-Gen3(8.0 GT/s). Fig. 1 shows the frequency response of CTLE for several  $A_{DC}$  values with 1.0 dB steps. Compensation inverts the effect of the channel by decreasing the gain of the low-frequency component with respect to the high-frequency one.

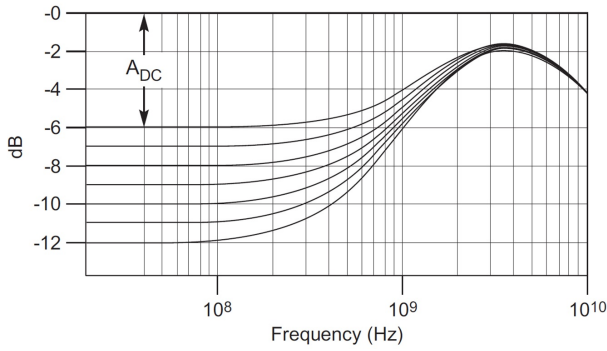


Figure 1. Frequency response of CTLE for PCIe-Gen3 (8GT/s) [8] for several  $A_{DC}$ .

### B. Feed-Forward Equalizer (FFE)

FFE is a 3-tap FIR filter. Fig.2 shows a realization of the filter. The behavior of the filter depends on the 3 taps coefficient values  $C_{-1}$ ,  $C_0$ , and  $C_{+1}$  as a weighted sum for the current input, the previous input and next bits values. The output from the filter is illustrated by (2).

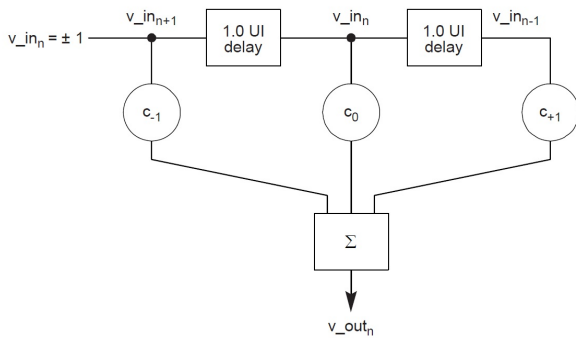


Figure 2. Realization of FFE as a 3-taps FIR filter [8].

$$v\_out_n = v\_in_{n+1} \times C_{-1} + v\_in_n \times C_0 + v\_in_{n-1} \times C_{+1} \quad (2)$$

where:

- $C_{-1}$ : gain of the first FIR tap (previous bit)
- $C_0$ : gain of the second FIR tap (current bit)
- $C_{+1}$ : gain of the third FIR tap (next bit)

The three coefficients can produce many combinations based on the used precession. However, some of these combinations are invalid. For example, it is not expected to produce a huge attenuation at the DC-level or use small range of the output swing. Therefore, followings are the constraints on FFE filter coefficients imposed by PCIe-Gen3 specifications to ensure that output signals will not violate minimum and maximum swing

relationship.

- $C_{+1} \leq 0$
- $C_{-1} \leq 0$
- $|C_{-1}| + |C_0| + |C_{+1}| = FS$
- $C_0 + |C_{-1}| + |C_{+1}| \geq LF$
- $|C_{-1}| \leq FS/4$

where:

- FS: Full swing value (FS = 1, for normalization)
- LF: low frequency value

Some constraints are used to ensure that the values of  $C_{-1}$ ,  $C_0$ , and  $C_{+1}$  are able to compensate the channel effect on high frequency. The low frequency components occur if several consecutive bits are similar. On the other hand high frequency components occur If the current bit is different than the previous and next bits. As shown in Fig. 3,  $V_d$  represents the maximum swing that occurs if the current bit is not equal the previous and next bit and can be determined by (3).  $V_b$  is the minimum output that occurs when current bit is same as previous and next bits and can be obtained by (4).  $V_a$  occurs when current bit is different than previous bit and same as next bit and can be obtained by (5).  $V_c$  occurs when current bit is different than next bit and same as previous bit and can be obtained by (6).

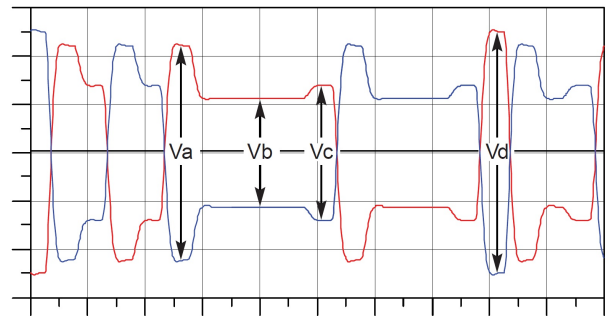


Figure 3. FFE effects on output voltage level [8].

$$V_d = -C_{-1} + C_0 - C_{+1} \quad (3)$$

$$V_b = C_{-1} + C_0 + C_{+1} \quad (4)$$

$$V_a = -C_{-1} + C_0 + C_{+1} \quad (5)$$

$$V_c = C_{-1} + C_0 - C_{+1} \quad (6)$$

The ratio between  $C_{-1}$ ,  $C_0$ , and  $C_{+1}$  define the de-emphasis boost and pre-shoot values of the transmitter

signal as illustrated in (7), (8) and (9). The effect of de-emphasis and preshoot on the waveform with part from compliance pattern 64-ones/64-zeros sequence are illustrated in Fig. 4 and Fig. 5

$$De - emphasis = 20 \times \log_{10}(V_b/V_a) \quad (7)$$

$$Preshoot = 20 \times \log_{10}(V_c/V_b) \quad (8)$$

$$boost = 20 \times \log_{10}(V_d/V_b) \quad (9)$$

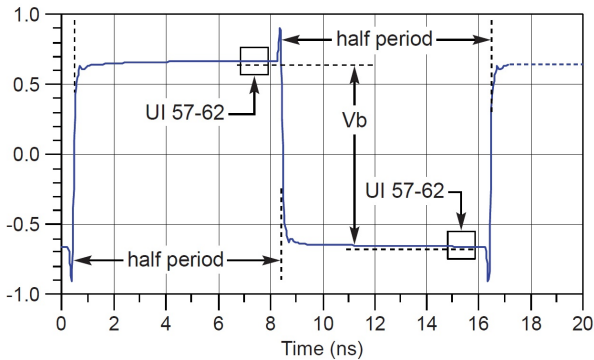


Figure 4. The effect of Preshoot only on compliance pattern [8].

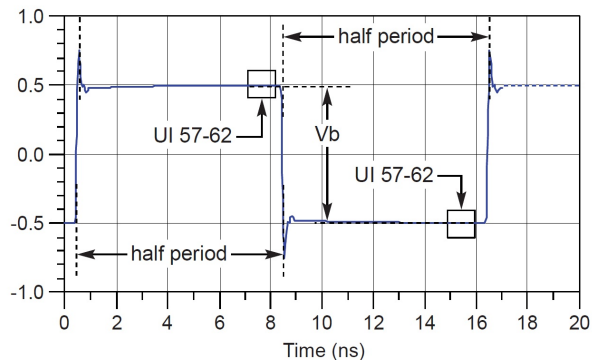


Figure 5. The effect of De-emphasis only on compliance pattern [8].

As shown in Fig. 4, the effect of preshoot appears on the current bit when the current bit and next bit are different. While the effect of de-emphasis is illustrated in Fig. 5 for the current bit when the current bit and previous bit are different. Both preshoot and de-emphasis increase the amplitude at bit transition, which contain the high frequency component of the signal. By increasing the amplitude, the channel deformation can be compensated. Based on the meaning of preshoot and de-emphasis PCIe-specifications set preset values to cover a wide-range of channels to be used for equalization to speedup the equalization process at start-up, as shown in Table I.

TABLE I. Preset values for FFE based on PCIe-specifications [8].

Preset No.	Preshoot (dB)	De-emphasis (dB)	C <sub>-1</sub>	C <sub>+1</sub>
P4	0	0	0	0
P1	0	-3.5 ± 1	0	-0.167
P0	0	-6.0 ± 1.5	0	-0.25
P9	3.5 ± 1	0	-0.166	0
P8	3.5±1	-3.5±1	-0.125	-0.125
P7	3.5±1	-6.0 ± 1.5	-0.100	-0.2
P5	1.9 ± 1	0	-0.1	0
P6	2.5 ± 1	0	-0.125	0
P3	0	-2.5 ± 1	0	-0.125
P2	0	-4.4 ± 1.5	0	-0.2
P10	0	Note <sup>1</sup>	0	Note <sup>1</sup>

Note 1: P10 is used for maximum boost  $C_{+1} = \frac{FS-LF}{2}$

### 3. RELATED WORK

The PCIe protocol is used in industry with many applications. Several research focused on PCIe to enhance signal integrity by adjusting several equalizers on transmitter and receiver sides. FFE is added on transmitter side and CTLE, and DFE are added at receiver sides. The PCIe connector has some specifications that affect the channel characteristics. Researchers focused on the enhancement of all parts that affect the channel characteristics. The enhancement can be obtained by changing the architecture to get better effect, by enhancing the adaptation method to achieve the best effect, by adding some constrains on the connector.

In [9], an analysis for the connector specifications is presented, specially for noise coupling mechanism by propose a new approach for the PCIe connector. On addition, a design of a 3-tap FFE in 16nm CMOS technology for highly flexible voltage-mode transmitter is developed in [10] that allows independent control of swing common-mode and equalization. A new implementation is provided in [4] for Continuous-Time Feed-Forward Equalizer (CT-FFE) to improve the sensitivity and remove the Inter-Symbol Interference (ISI). The CT-FFE is implemented with first order filter. With high-rate data transmission on optical communication, an 8-tap FFE is designed in [5]. In [11], a realization of CTLE for high speed receiver is implemented using 28nm CMOS technology.

Researchers also focused on the adaptation of the equalizers. In [1], an adaptive CTLE is proposed based on spectrum balancing with a frequency detector to increase the equalizer bandwidth. In [2], an Asynchronous Feedback Continuous-Time Linear Equalizer (AF-CTLE) is implemented and adapted with a 3-step eye detection algorithm to reduce power consumption. In [3], a design for CTLE is presented with adaptation for its parameters to decide the placement of poles and zeros to create an



efficient CTLE.

In [12], a new method for obtaining an optimal configuration for FFE and DFE is presented by finding the coefficients for both equalizers simultaneously. In [6], an N-tap decision feedback equalizer is proposed to enhance the signal integrity based on a statistical eye-diagram estimation. A direct DFE is presented in [7] for a high-speed operation with enhancement of the DFE delay by avoiding the first tap weighting transistors.

The remaining sections of this paper are organized as following. Section 4 makes an analysis for FFE in frequency domain. Section 5 suggests new preset values based on the frequency domain analysis. Section 6 shows the mathematical model for short and long channel based on the PCIe-standard criteria. Results is presented on Section 7 with a comparison between the Preset in standard and suggested values. Finally, conclusion and future work are included in Section 8.

**4. FREQUENCY DOMAIN ANALYSIS OF FFE**

FFE settings are described in PCIe-Gen3 based on the time domain parameter de-emphasis, pre-shoot, and boost. This section illustrates the effect of FFE on the frequency domain and shows the method that can be used based on frequency domain parameters to select the best FFE settings with respect to channel behavior. The analysis starts by (10) to calculate the Z-transform for (2). Equation (11) can be used to map from z-domain to s-domain approximately. Equation 12 approximately represents the (10) in s-domain

$$Vout(Z) = (C_{-1}Z^1 + C_0 + C_+Z^{-1})Vin(Z)$$

$$G(z) = \frac{Vout(Z)}{Vin(Z)} = C_{-1}Z^1 + C_0 + C_+Z^{-1} \tag{10}$$

$$Z = e^{sT} = e^{s\frac{T}{2}} \times e^{s\frac{T}{2}} = \frac{e^{s\frac{T}{2}}}{e^{-s\frac{T}{2}}} \cong \frac{1 + s\frac{T}{2}}{1 - s\frac{T}{2}} \tag{11}$$

$$G(s) = C_{-1} \frac{1 + s\frac{T}{2}}{1 - s\frac{T}{2}} + C_0 + C_+ \frac{1 - s\frac{T}{2}}{1 + s\frac{T}{2}} \tag{12}$$

By simplification and the following substitution:

Maximum output=  $FS = 1 = -C_{-1} + C_0 - C_+$

Minimum output=  $LF = \alpha FS$

$LF = C_{-1} + C_0 + C_+, 0 \leq \alpha \leq 1$

We get:

$$G(s) = \alpha \left[ \frac{\left(1 + \left(\frac{C_{-1}-C_+}{\alpha}\right)Ts - \left(\frac{T^2}{4\alpha}\right)s^2\right)}{\left(1 - s^2\frac{T^2}{4}\right)} \right] \tag{13}$$

$$G(s) = A_{DC} \left[ \frac{1 + \left(\frac{2\zeta}{\omega_z}\right)s - \left(\frac{s}{\omega_z}\right)^2}{1 - \left(\frac{s}{\omega_p}\right)^2} \right] \tag{14}$$

where:

DC-Gain:  $A_{DC} = \alpha$

Damping ratio:  $\zeta = \frac{C_{-1}-C_+}{\sqrt{\alpha}}$

Pole frequency:  $\omega_p = \frac{2}{T}$

Zero frequency:  $\omega_z = \frac{2}{T} \sqrt{\alpha}$

As shown in (13) and (14), the transfer function has two poles at  $\omega_p$  and two zeros at  $\omega_z$  with  $\omega_z < \omega_p$ , as  $\alpha < 1$ . The damping ratio  $\zeta$  depends on the difference between  $C_{-1}$  and  $C_+$ .

Fig. 6 and Fig. 7 show the frequency response for (14) based on frequency domain analysis. Fig. 6 shows the effect of  $\alpha$  on the attenuation at low frequency and Fig. 7 shows the effect of  $\zeta$  with constant  $\alpha = -10$  dB on the shape of the frequency response.

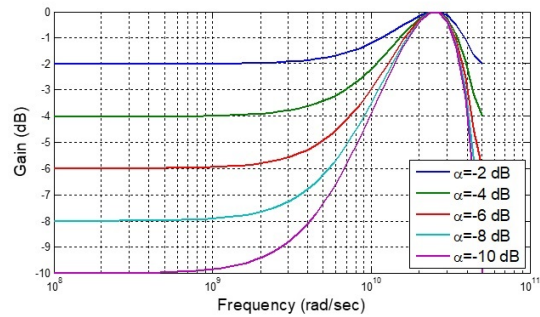


Figure 6. Frequency response of FFE with different attenuation ( $\alpha$ ).

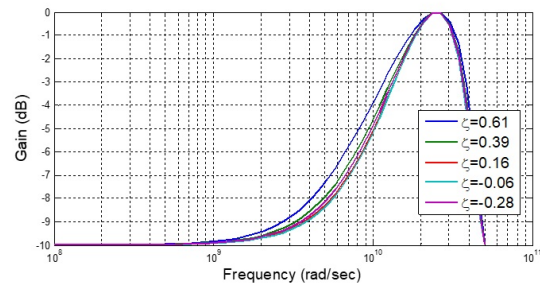


Figure 7. Frequency response of FFE with different damping ratio ( $\zeta$ ).

Based on the frequency analysis for the FFE, several responses can be used for a specific  $\alpha$  with different damping ratio  $\zeta$ . Table II shows  $\zeta$  and  $\alpha$  for Preset value specified by PCIe-standard and ordered by  $\alpha$ . As shown in Table II, the attenuation ( $\alpha$ ) covers the range from 0 to -7.96 dB.

Also, some attenuation values are repeated with different  $\zeta$  as (P3, P6), (P1, P9), and (P0, P8). Based on this analysis the optimal value can be obtained by search on the nearest  $\alpha$  and  $\zeta$ . For example. If the best FOM occurs



with P2, the search should be focus around  $\alpha$  equal to -4.44 dB,  $\zeta$  equal to 0.26.

TABLE II. Preset ratio for FFE based on standard with ( $\zeta$  and  $\alpha$ ).

Preset No.	$C_{-1}$	$C_{+1}$	$\zeta$	$\alpha(\text{dB})$
P4	0	0	0	0
P5	-0.1	0	-0.11	-1.94
P6	-0.13	0	-0.14	-2.5
P3	0	-0.13	0.14	-2.5
P1	0	-0.17	0.2	-3.48
P9	-0.17	0	-0.2	-3.48
P2	0	-0.2	0.26	-4.44
P0	0	-0.25	0.35	-6.02
P8	-0.13	-0.13	0	-6.02
P7	-0.1	-0.2	0.16	-7.96

5. RECOMMENDED PRESET VALUES

As illustrated before, the FFE settings are defined based on  $\alpha$  and  $\zeta$ . Based on PCIe-specifications, some constraints should be considered as illustrated in Section 1 and the FFE’s frequency domain parameters. The following items summarize these constraints.

- Maximum swing ratio at high frequency equal 1
  - $-C_{-1} + C_0 + C_{+1} = 1$
- Minimum swing ratio at low frequency=  $\alpha$ 
  - $C_{-1} + C_0 + C_{+1} = \alpha$
- $C_0 = \frac{\alpha+1}{2}$
- $C_{+1} = \frac{\alpha-1}{2} - C_{-1}$
- Let  $C_{-1} = \frac{\gamma}{4}$ 
  - where  $0 \leq \gamma \leq 1$
- As  $C_{+1} \leq 0 \Rightarrow \frac{\alpha-1}{2} - C_{-1} \leq 0$
- Let  $C_{-1} = \frac{\gamma}{4}$ , where  $0 \leq \gamma \leq 1$
- Therefore,  $\frac{\alpha-1}{2} - C_{-1} + \frac{\gamma}{4} \leq 0$
- i.e.,  $\min[1, 2(1 - \alpha)] \geq \gamma \geq 0$

Based on the above constraints, new preset values are generated in Table III for full attenuation range as specified in the PCIe-Gen3 standard ( $-1.94\text{dB} \leq \alpha \leq -7.96\text{dB}$ ). But, with minimum and maximum values for  $\zeta$  to get all possible cases.

TABLE III. Suggested preset values.

Preset No.	$C_{-1}$	$C_{+1}$	$\zeta$	$\alpha(\text{dB})$
SP0	0	0	0	0
SP1	0	-0.1	0.11	-1.94
SP2	-0.1	0	-0.11	-1.94
SP3	0	-0.15	0.18	-3.1
SP4	-0.15	0	-0.18	-3.1
SP5	0	-0.2	0.26	-4.44
SP6	-0.2	0	-0.26	-4.44
SP7	0	-0.25	0.35	-6.02
SP8	-0.25	0	-0.35	-6.02
SP9	0	-0.3	0.47	-7.96
SP10	-0.25	-0.05	-0.32	-7.96

6. MATHEMATICAL-MODEL FOR SHORT AND LONG CHANNELS

The mathematical-model for short and long channels is shown in Fig. 8. The PCIe specifications define the attenuation at 1 GHz and 4 GHz as follows:

- Short channel @ 1 GHz:  $-4 \pm 1$  dB
- Short channel @ 4 GHz:  $-12 \pm 2$  dB
- Long channel @ 1 GHz:  $-6.5 \pm 1.5$  dB
- Long channel @ 4 GHz:  $-20 \pm 2$  dB

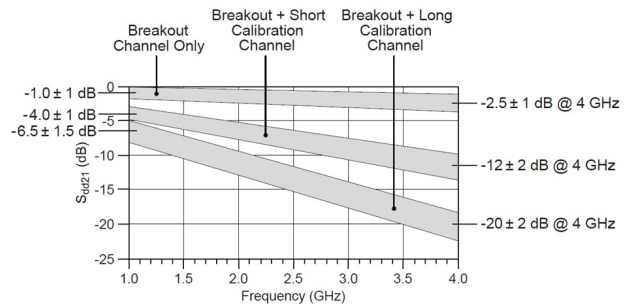


Figure 8. Attenuation limits for short and long channel [8].

The difference between the two corners (1 GHz and 4 GHz) is two octaves. However, each pole/zero produces 6 dB/octave. Therefore, for a short channel, the difference between low and high attenuation is less than 12 dB. Two poles can be used to achieve each attenuation and one zero between them compensates the effect of the first one, as given by (15). For a long channel, the difference between the two attenuation is larger than 12 dB. Therefore, two





poles can be used to achieve the required attenuation at each frequency, as given by (16).

$$H_{short}(s) = \frac{\left(1 + \frac{s}{\omega_2}\right)}{\left(1 + \frac{s}{\omega_3}\right)\left(1 + \frac{s}{\omega_4}\right)} \quad (15)$$

$$H_{long}(s) = \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \quad (16)$$

Equations (15) and (16) are used with channel specifications to calculate the channel-model parameters as follows:

- Short channel:
  - $\omega_1 = 4.29 \times 10^9 \text{ rad/sec}$
  - $\omega_2 = 6.28 \times 10^9 \text{ rad/sec}$
  - $\omega_3 = 1.06 \times 10^{10} \text{ rad/sec}$
- Long channel:
  - $\omega_1 = 3.3 \times 10^9 \text{ rad/sec}$
  - $\omega_2 = 6.3 \times 10^9 \text{ rad/sec}$

Fig. 9 and Fig. 10 show the frequency response for short and long channels, respectively based on the calculated values to match the specifications for a worst channel.

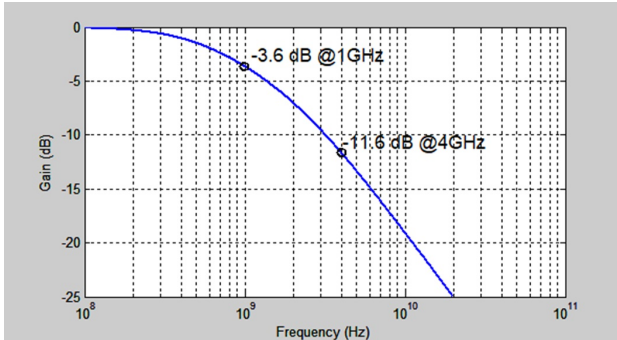


Figure 9. Frequency response for short channel.

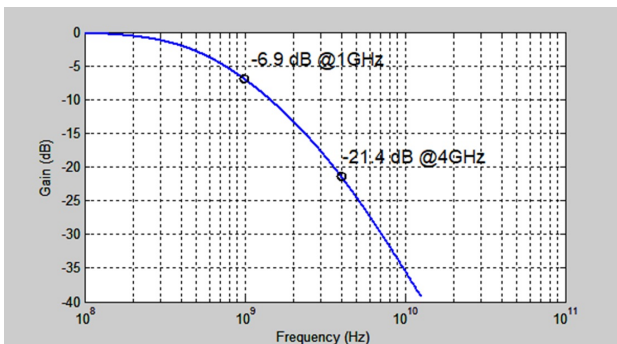


Figure 10. Frequency response for long channel.

## 7. EXPERIMENTAL RESULTS

Long and short channels are used to evaluate the proposed presets and compare the obtained eye-diagram in each case. The FOM of the eye-diagram is measured in this research by computing the difference in area after the slicer output with several thresholds. Eight slicers are used to evaluate the FOM as illustrated below:

- larger than 0
  - Slicer S1: check for values  $> 0$
  - Slicer S2: check for values  $> 20\%$
  - Slicer S3: check for values  $> 50\%$
  - Slicer S4: check for values  $> 90\%$
- less than 0
  - Slicer S5: check for values  $< 0$
  - Slicer S6: check for values  $< -20\%$
  - Slicer S7: check for values  $< -50\%$
  - Slicer S8: check for values  $< -90\%$
- Fitness =  $\frac{1}{2} \times \left[ \sum_{i=2}^4 \left( \frac{S_0 - S_i}{S_0} + \frac{S_5 - S_{(4+i)}}{S_5} \right) \right]$

Note: eye-opening is increased by minimizing the fitness function

As the CTLE is able to enhance the channel characteristics, to ensure that the suggested value will cover all possible case, Tables IV and V show the calculated fitness function for preset values by the specifications and the suggested presets and the enhancement percentages.

Positive value in the percentages is an indication of the benefit of the suggested preset. However, negative values indicate that the specifications preset is better than the suggested one. The only negative number occurs with short channel at  $A_{DC} = -5$  dB, (the difference between suggested preset compared to the specifications is very small as the enhancement percentage is  $-1.2\%$ ). On the other hand, the enhancement percentage using suggested preset are about  $8.3\%$  in long channel and  $10.9\%$  on short channel.

To illustrate the enhancement percentage  $8.3\%$  using long channel, Fig. 11 shows the best eye-diagram that can be obtained with PCIe-standard preset values. Fig 12 Shows the best eye-diagram can be obtained with suggested preset values. The eye-diagram with suggested preset value is more opened compared to using preset value with PCIe-standard.

To obtain more enhanced eye-diagram, it is recommended to check all values neighbor to the best preset value that are obtained from PCIe-specifications or the suggested ones after calculating the frequency domain parameters ( $\alpha$ ,  $\zeta$ , or  $\gamma$ ). The preset values cannot cover all possible cases. However, using pre-defined preset values, the nearest optimal value can be obtained in short-time.

TABLE IV. Percentage of the enhancement between standard and suggested preset values for long channel.

$A_{DC}$ (dB)	Preset		Enhancement (%)
	(Suggested)	(Spec.)	
-1	0.596	0.602	1
-2	0.586	0.607	3.6
-3	0.572	0.594	3.8
-4	0.556	0.578	4
-5	0.538	0.56	4.1
-6	0.518	0.54	4.2
-7	0.497	0.52	4.6
-8	0.473	0.499	5.5
-9	0.44	0.475	8
<b>-10</b>	<b>0.422</b>	<b>0.457</b>	<b>8.3</b>
-11	0.424	0.442	4.2
-12	0.425	0.438	3.1
-13	0.448	0.45	0.4
-14	0.457	0.459	0.4

TABLE V. Percentage of the enhancement between standard and suggested preset values for short channel.

$A_{DC}$ (dB)	Preset		Enhancement (%)
	(Suggested)	(Spec.)	
<b>-1</b>	<b>0.416</b>	<b>0.459</b>	<b>10.3</b>
<b>-2</b>	<b>0.402</b>	<b>0.446</b>	<b>10.9</b>
-3	0.415	0.435	4.8
-4	0.401	0.421	5
<b>-5</b>	<b>0.41</b>	<b>0.405</b>	<b>-1.2</b>
-6	0.396	0.408	3
-7	0.402	0.414	3
-8	0.394	0.418	6.1
-9	0.415	0.42	1.2
-10	0.418	0.423	1.2
-11	0.421	0.424	0.7
-12	0.425	0.427	0.5
-13	0.427	0.441	3.3
-14	0.431	0.462	7.2

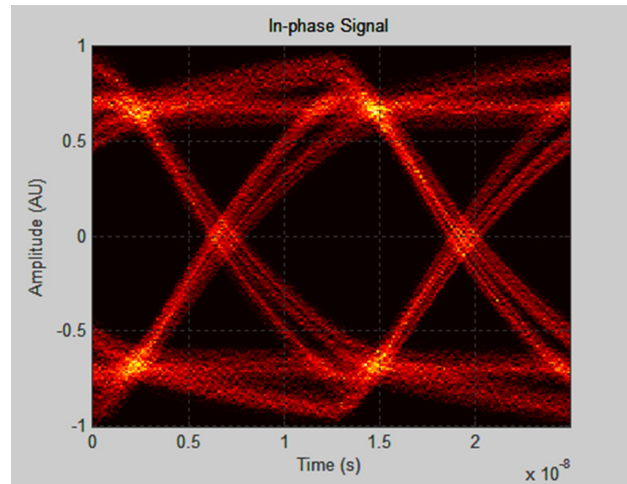


Figure 11. Best Eye-diagram for long channel with  $A_{DC}=-10$  dB with PCIe specifications preset values.

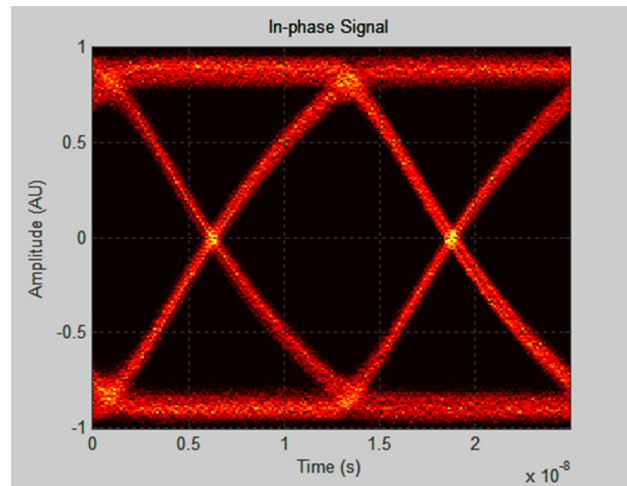


Figure 12. Best Eye-diagram for long channel with  $A_{DC}=-10$  dB with suggested preset values.

### 8. CONCLUSION AND FUTURE WORK

This research provides an analysis of FFE in frequency domain. Based on this analysis new preset values are suggested to cover all possible range for different channels. Mapping the best preset value to frequency domain parameters, will help to find optimal FFE settings by check all neighbor values of the obtained preset value. The experimental results show that new suggested preset values are better than preset values that are defined by PCIe-standard specifications for worst short and long channels with different CTLE boost values. As an enhancement it is better to use an intelligent search technique to find the best FFE settings by searching all possible plane in a reasonable time.



## REFERENCES

- [1] C. Cai, Y. Zhou, and J. Zhao, "5–20 Gbit/s adaptive CTLE with spectrum balancing method," *Electronics Letters*, vol. 54, no. 5, pp. 274–276, Aug. 2018.
- [2] M. Kim, J. Chae, S. Choi, G. Hong, H. Ko, D. Jeong, and S. Kim, "A 4266 Mb/s/pin LPDDR4 Interface With an Asynchronous Feedback CTLE and An Adaptive 3-step Eye Detection Algorithm for Memory Controller," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 12, pp. 1894–1898, Dec. 2018.
- [3] T. Reuschel, J. B. Preibisch, and C. Schuster, "Efficient design of continuous time linear equalization for loss dominated digital links," in *2017 IEEE 21st Workshop on Signal and Power Integrity (SPI)*, May 2017, pp. 1–4.
- [4] M. Madani and G. E. R. Cowan, "10 Gb/s optical receiver with continuous-time feed-forward equalization," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2017, pp. 926–929.
- [5] C. Menolfi, M. Braendli, P. A. Francese, T. Morf, A. Cevrero, M. Kossel, L. Kull, D. Luu, I. Ozkaya, and T. Toifl, "A 112 Gb/s 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, Feb. 2018, pp. 104–106.
- [6] J. Park, H. Song, D. Kim, S. Choi, and J. Kim, "Statistical eye-diagram estimation method for high-speed channel with n-tap decision feedback equalizer (DFE)," in *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EM-C/APEMC)*, May 2018, pp. 1027–1032.
- [7] D. Lee, D. Lee, Y. Kim, and L. Kim, "A 0.9-V 12-Gb/s Two-FIR Tap Direct DFE With Feedback-Signal Common-Mode Control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 3, pp. 724–728, Mar. 2019.
- [8] "PCI Express Base Specification Revision 3.0," <https://members.pcisig.com/wg/PCI-SIG/document/download/8265> [Last visited on July 22nd, 2019], 2010.
- [9] Y. Zhou, W. Shi, and S. Sudhakaran, "A new approach to mitigate PCI express Gen4 crosstalk from sideband signals in connectors," in *2017 IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Oct. 2017, pp. 1–3.
- [10] K. L. Chan, K. H. Tan, Y. Frans, J. Im, P. Upadhyaya, S. W. Lim, A. Roldan, N. Narang, C. Y. Koay, H. Zhao, and K. Chang, "A 32.75-Gb/s voltage mode transmitter with 3-tap FFE in 16nm CMOS," in *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Nov. 2016, pp. 233–236.
- [11] V. S. Melikyan, A. V. Matevosyan, A. S. Petrosyan, A. A. Martirosyan, K. T. Khachikyan, R. H. Musayelyan, A. S. Trdatvan, and D. K. Hakobyan, "High quality factor 5.0 Gbps CTLE Circuit for SERDES Serial Links," in *2018 IEEE East-West Design Test Symposium (EWDTS)*, Sep. 2018, pp. 1–5.
- [12] N. Dikhaminjia, M. Tsiklauri, Z. Kiguradze, J. He, J. Drewniak, A. Chada, and B. Mutnury, "Combined Optimization of FFE and DFE Equalizations," in *2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, Oct. 2018, pp. 21–23.



**Ahmed M. Zaki** received the B.Sc. (Hons.), M.Sc., and Ph.D. degrees in systems engineering from Ain Shams University, Cairo, Egypt, in 2002, 2007, and 2012, respectively, where he is currently an Assistant Professor of systems engineering with the Department of Computer and Systems Engineering Department. His general research interests include digital signal processing, and control systems.