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Channel Length-Based Comparative Analysis of Temperature and Electrical Characteristics for SiNWT and GeNWT

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Abstract: This paper investigates the temperature sensitivity and electrical characteristics of Silicon Nanowire Transistor (SiNWT) and Germanium Nanowire Transistor (GeNWT) depending on variable channel length (Lg). It also studies the possibility of using them as a temperature nanosensor. The MuGFET simulation tool was exploited to investigate the characteristics of the considered nanowire transistors. Current-voltage characteristics with different values of temperature with channel length [Lg = 25, 45, 65, 85 and 105 nanometer (nm)], were simulated. MOS diode mode connection suggested measuring the temperature sensitivity of SiNWT and GeNWT too. Three (3) electrical characteristics namely; (i) Subthreshold Swing (SS), (ii) Threshold voltage (V_T), and (iii) Drain-induced barrier lowering (DIBL) were evaluated and compared for both NWTs. The obtained results show that SiNWT achieved a better temperature sensitivity with channel length range between 25 nm to 105 nm at operation voltage (V_{DD}) range 1 V to 5 V nm. It is very clear that the temperature sensitivity increased remarkably by increasing channel length for both of SiNWT and GeNWT as well, but in SiNWT the sensitivity is more steady compared to GeNWT that showing less sensitivity. Moreover, SiNWT shows better result in terms of electrical performance metrics for various channel length at T = 300 K comparing with GeNWT.

Keywords: SiNWTs; GeNWT; Channel length; Temperature sensitivity; Electrical characteristics.

1. INTRODUCTION

The improvement of new technology is described by its prominence on miniaturization scale to ultra-micro dimensions. That is the main principle of Nano technology which invaded the field of applied science, manufacturing, industrial, military, medical, agricultural and other fields[1-3] The most remarkable example for that is in nanoelectronics and nanoscience, where the technological progress has come from reductions, downsizing transistors and adding more numbers of transistors per chip [4, 5]. The scaling of the complementary metal-oxide-silicon (CMOS) does not track the constant-field scaling principle accurately because of non-scaling factors- the threshold voltage [6, 7]. The metal oxide semiconductor field effect transistors (MOSFET) are aiming at creating more sophisticated integrated circuits via using more transistors per chip. However, this was restricted by high-field effects on downscaled devices [5, 8]. Over the last four decades, experts and researchers had increased the intricacy of integrated circuits IC's thru further five orders of stages. That incredible reaching has changed the world. The downsizing of transistors to the nm region means to find out and investigating in the field of nanoscale materials and nanoscience as well. The nanometer has been as significant to science as the micrometer was in the previous century [9].

Major studies published recently in nanoscience and nanotechnologies have focused on the fabrication of numerous new nano apparatus and tools as well with a wide series of uses in electronics, biomaterials, medicine and power supplying [10, 11]. Many innovative devices structures have been extensively explored due to the classical MOSFET approaches its scaling limits. Amongst them, nanowire transistor (NWT) which has pulled a magnificent attention from researchers to both, academic and semi-conductor industry as well [12, 13]. In nanoelectronics research, nanowire is very important to be considered and studied as well for the purpose of designed as a nano transistor for many functions. Nanowire is a spherical or quadrangular intersected nanostructure where a thickness or diameter is designated to lots of nanometers or fewer and an undesignated length. Various altered types of nanowires were proposed including metal, semiconducting, and isolating, for

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electronic scheme uses. In nano electronics exploration, a semiconducting nanowire is used in active devices, an isolating nanowire is used in nano-capacitors, and a metallic nanowire is used to connect nano-formed into particularly small circuits [14]. In order to generate dynamic electronic devices, an essential step is to dope a semiconductor nanowire to generate p-type and n-type semiconductors. This process has already been performed on individual nanowires [15]. The next step is to produce a p-n junction nanowire-diode, which is the easiest amongst electronic devices. This process was conducted by either physically crossing a p-type wire over an n-type wire or doping a single wire with different dopants along the length of the wire or radially [16, 17].

Among various sensing and monitoring techniques, sensors based on field effect transistors (FETs) have attracted considerable attention from both industry and academia. Owing to their unique characteristics such as small size, light weight, low cost, flexibility, fast response, stability, and ability for further downscaling, nanowire field effect transistor (NW-FET) can serve as an ideal nanosensor. It is the most likely successor to FET-based nanoscale devices. However, as the dimensions (channel length and diameter) of NWT channel are shrinking down, electrical and temperature characteristics of NWTs should be affected, thereby degrading transistor performance. Although applications of NWTs as biological and/or chemical sensors have been extensively explored in the literature, less attention has been devoted to utilize such transistors as temperature sensors.

Consequently, this study aims to investigate, compare and analyze the impact of channel length of two NWTs namely; SiNWT and GeNWT N-Types, as the most commonly used NWTs, on their electrical and temperature characteristics. Accordingly, design of a temperature nanosensor for enabling continuous temperature monitoring with superior detection capabilities, high flexibility, and low-cost can be achieved. To fulfil these objectives, the current study adopted the following methodology and contributions:

- Analysing the impact of channel length of both SiNWT and GeNWT on their electrical and temperature characteristics.
- Selection of optimal channel length for both types based on comparison of transistors performance.
- Design a NWT-based temperature nanosensor depending on constituent semiconductor materials for enhancement of temperature stability and sensitivity.

The remaining part of this paper is structured as follows: The next section presents related studies with an overview of Nanowire technology. Section III introduces adopted methods of this research. The results and discussions are presented in Section IV. Finally, paper is concluded in Section V.

2. RELATED WORKS

Electronic devices in Nano dimension such as diodes, transistors, capacitors and resistors appealing, particularly the attention to the electronics industry due to the drive for ever-smaller electronic circuits. The ideas of nanotechnology emanated long ago from the concept promulgated by Richard Feynman. In his description of the concept put forward a scenario in which researchers can manipulate and control materials at atomic and molecular level [18]. The emergence of a scanning tunnelling microscope in 1981 clearly revealed the application of nanoscience for individual atoms at a molecular level [17]. Nanotechnology is therefore defined as the manipulation of atomic matter on a molecular and super-molecular level [19] reported the molecular nanotechnology as the atomic or molecular manipulation which results in the fabrication of products on a macro scale. The National Nanotechnology Institute (NNI) further provided a generalized description of nanotech as the manipulation of matter with at least 1-dimension sized from one to hundred nanometres. This definition is a total deviation from the traditional technological point-of-view to a more research-oriented category, which deals primarily with the special properties of matter below a certain size threshold. It is a common practice therefore to pluralize this miniaturization as form “nanotechnologies” as well as “Nano-scale technologies”. The application of nanoscience and its inherent technology has been extensively used in interdisciplinary research most especially for the past two decades. This indicated a wide range of research applications with size as the target variable. Many countries have therefore invested more in nanotechnology-related research due to several potential military and industrial applications.

The concept of nanotechnology involves the use of low dimensional materials with different structural configurations which include the nanowires, nano-rods, nanotubes or nano-crystalline films [20]. A nanowire in electronics engineering is a circular or rectangular cross-sectional nanostructure that has a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. Numerous different types of nanowires exist, including metallic, semiconducting, and insulating, for electronic device applications. All of these types are important. In nano electronics research, a semiconducting nanowire is used in active devices, an insulating nanowire is used in nano-capacitors, and a metallic nanowire is used to link nano-components into extremely small circuits. In order to optimize dimensions, ambient temperature and orientation of channel in SiNWT and GeNWT design, simulation is needed to characterize the behavior of the NWT and help making design decisions.

The transistor based temperature sensors are designed depending on the temperature characteristics of current-voltage curves of the Nanowire transistor [21, 22]. The bipolar transistor can be used as a temperature sensor by connecting the base and collector together. This will use a transistor in diode mode. While the transistor in MOSFET

structures can be used as a temperature sensor by connecting the gate with either source or drain.

Simulating the characterisation of FinFET behaviour and helping in decision-making is necessary to reduce channel dimensions and improve the performance in FinFET design. Some of the studies discussed one-channel dimension length or width or oxide thickness, for example, depending on one property such as V_T or SS or DIBL only and for one semiconductor type such as Ge-FinFET or Si-FinFET. The FinFET as a temperature nano-sensor based on channel semiconductor type was investigated by [23]. The temperature sensitivity of FinFET (with Si Ge GaAs and InAs) was simulated as a semiconductor channel. FinFET transfer properties with V_D = 1V were studied at different operating temperature values (-25, 0, 25, 50, 75, 100 and 125 °C) for all semiconductor channel types. The results showed that FinFET is best used as a nano-sensor with GaAs. However, the study only focused on FinFET types of transistor and none of nanowire transistors.

In [24], authors carried out an evaluation and comparison study between SiNWT and planer MOSFET depending on I_{ON}/I_{OFF} ratio and SS, and that led to fabricated the SiNWT devices with rectangular cross-section of thin silicon-on-insulator nanowires, 10 nm thick and 30 nm wide, these transistor devices attained I_{ON}/I_{OFF} ratios of 10^6 with SS close to the idyllic MOSFET limit of 60 mV/decade at room temperature, which is the superlative performance so far in the gated-resistor device assembly. Nevertheless, temperature stability was not considered. In addition, only SiNWT was evaluated and not GeNWT.

Ref. [25] simulated the temperature effects on the transfer (Id-Vg) characteristics of SNWT at Vd=1V with diverse values of temperature (275, 300, 325, 350 and 375 K). Authors claimed that current- regulated to diameter-increased with increasing temperature at low Vg (>0.4V) and reducing at high Vg (<0.4V). Additional to that it can be recorded that changing in an operational temperature lead to change in ON current to OFF current ratio (I_{ON}/I_{OFF}), threshold voltage (V_T), DBIL and SS. However, the study did not consider GeNWT and only electrical characteristics were evaluated.

To the best of our knowledge, few studies investigated the effects of channel dimensions of NWT on the temperature characteristics and electrical characteristics simultaneously. Some studies focused more on electrical characteristics of NWT while others considered temperature characteristics of other types of transistors such as FinFET. Few related literatures focused on SiNWT and none of existing studies investigated GeNWT based on channel length and temperature variation. This study considered two types of nanowire transistors (SiNWT and GeNWT). In addition, it evaluates and compares their performance based on both electrical and temperature characteristics. It is among the limited number of studies that focused on the application of nanowire transistor as a temperature nanosensor. Unlike the previous studies that considered only one parameter in their evaluation, this paper analyses the impact of several parameters on the transistors performance simultaneously. In particular, the effect of varying channel length, operating voltages (V_{DD} and V_g), ambient temperature, and semiconductor material (Si and Ge) all were considered.

3. METHODS AND MATERIALS

After reviewing relevant literature and highlighting limitations in the field of nanotechnology applications, thus identifying problem statement of this research, FOUR (4) main phases were adopted for the general descriptive research methodology. These phases include different stages and research activities in conjunction with the detailed simulation environment. In addition, it clarifies the simulation procedures to investigate and analyze transistor performance as a temperature nanosensor.

(i) Phase I–. Considering Nanowire transistor as the most likely successor to FinFET-based nanoscale devices, and selecting the well-known MUGFET Simulator as the simulation tools to conduct this study due to its superiority and reliability in simulating and characterizing field effect transistors;

(ii) Phase II– Developing an analytical framework to analyze the effect of channel length on the performance of Silicon Nanowire transistor (SiNWT) and Germanium nanowire transistor (GeNWT) on their electrical and temperature characteristics;

(iii) Phase III– Accordingly, selection of NWTs optimal channel length by considering temperature sensitivity and electrical characteristics (SS, V_{TH}, and DIBL).

A. Simulation Setup

MuGFET simulator is utilized in this study for the analysis of temperature characteristics for SiNWT and GeNWT based on channel length. Simulation tools of electronic devices have become increasingly important to understand the physics behind the structures of new devices. Simulation tools can also help to identify device strengths, weaknesses, and retrenchment costs and illustrate the extensibility of these devices in the nm range. This software provides many useful characteristic curves for both nanowires and FinFET for deeply understanding Physics.

TABLE I. SIMULATION PARAMETERS

Parameters	value
Channel length (Lg)	(25, 45, 65, 85 and 105) nm
Channel diameter (D)	40 nm
Oxide thickness (T_{OX})	2.5 nm
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}

The output characteristic curves of the transistor under different conditions and with different parameters that can be extracted from the simulator. MuGFET simulator also provides self-consistent solutions to the Poisson and drift-diffusion equation. It is used to simulate the motion of transport objects in the calculation of the characteristics for Nanowire. Basically, experimental work can be supported by simulation studies to further explore the development of MuGFET for Nano-dimensional characterization.

In our simulations, the I_d-V_g characteristics of NWTs at a temperature (250, 275, 300, 325, 350, 375, 400, 425 and 450 K) were simulated with Channel diameter = 40 nm for different channel lengths and operating voltages. Both semiconductor materials were considered, Si and Ge. In this case, for each channel length, twenty-one (21) operating voltages (V_{DD}) in the range 0-5 V were considered by step of 0.25 V. Details simulation parameters are listed in Table I.

B. Temperature Sensitivity

Temperature sensitivity is a performance metric that measure the changes in transistor behavior by varying operating voltages and surrounding temperature. It depends on the variation of drain current, ΔI_d. Delta is used to measure and observe the drain current I_d where simulation results arranging many matrices according to Vg as a function of I_d. It can be calculated by subtract the small value of Id from the bigger one by using the following linear equation:

$$\Delta I_d = I_{dn} - I_{d(n-1)} \qquad (1)$$

The different values of temperature (225, 250, 275, 300, 325, 350, 375, 400, 425 and 450 K) effects on SiNWT and GeNWT characteristics were studied with different channel lengths (Lg = 25, 45, 65, 85 and 105 nm). For the diode mode transistor connection, the increments in current (ΔI_d) with temperature will occurred by increasing of channel length and temperature for both transistors and SiNWT and GeNWT.

4. SIMULATION RESULTS

A. SiNWT Performance

In the first simulation scenario, the Id–Vg characteristics of SiNWT for varying temperatures from 250 to 450 K by increasing of 25 K were simulated. Figure 1 to Figure. 5 show the change in ΔI_d, as an indicator of transistor sensitivity with temperature variation for each Lg value (25, 45, 65, 85, and 105 nm) respectively. The V_{DD} also varied in the range of 0 – 5 V at 0.25 V steps. For the sake of figures clarity, only 6 voltage values are selected (two max., two min. and two medium). Other obtained values for the rest voltages are distributed between the maximum and minimum. It is obvious that the maximum sensitivities (max ΔI_d) obtained at the relatively lower temperatures, and the values decreased linearly as temperature increased for all V_{DD} voltages. Our aim in this scenario is to find the highest sensitivity for various operating voltage and various channel length. For SiNWT, the maximum temperature sensitivity values are obtained at V_{DD} = 0.75 V for Lg = 25 nm; followed by max ΔI_d at V_{DD} = 1.5 V for L_g = 45 nm, V_{DD} = 2 V for L_g = 65 nm, V_{DD} = 2.25 V for L_g = 85 nm, and finally V_{DD} = 2.5 V for L_g = 105 nm.

From the obtained simulation results, maximum sensitivities (max ΔI_d) were observed at lower V_{DD} voltages with short channel lengths (25 to 45 nm) while at longer channel length, the highest sensitivity was achieved with higher values of operating voltages. For the sake of brevity, in this paper we only highlight the highest obtained temperature sensitivity based on channel length. Figure 6 shows the changes in ΔI_d with increasing V_{DD} at various temperatures for 105 nm channel length. As shown in the figures, the maximum sensitivity of 5.73×10^{-5} was achieved at 2.5 volts. The sensitivity was smaller at higher and lower operating voltages. The sensitivity also inversely proportional to the ambient temperature. The highest temperature sensitivity of SiNWT was achieved at the lowest operating temperature, 250 K.

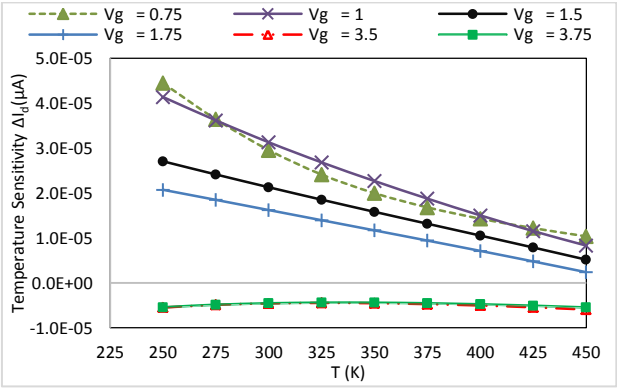

Figure 1. Temperature characteristics of SiNWT at Lg = 25 nm

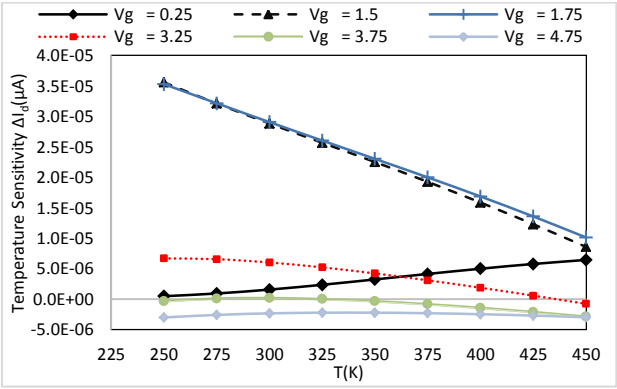

Figure 2. Temperature characteristics of SiNWT at Lg = 45 nm

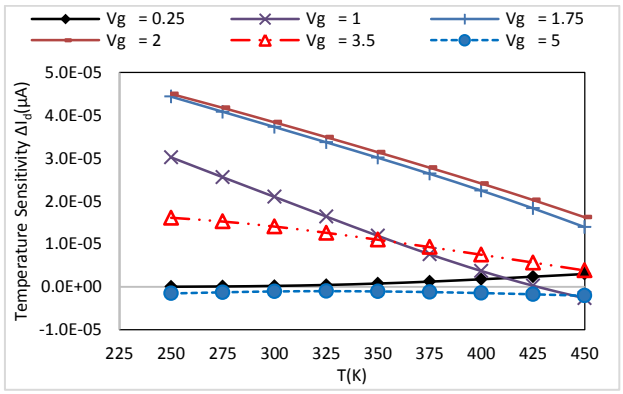

Figure 3. Temperature characteristics of SiNWT at Lg = 65 nm

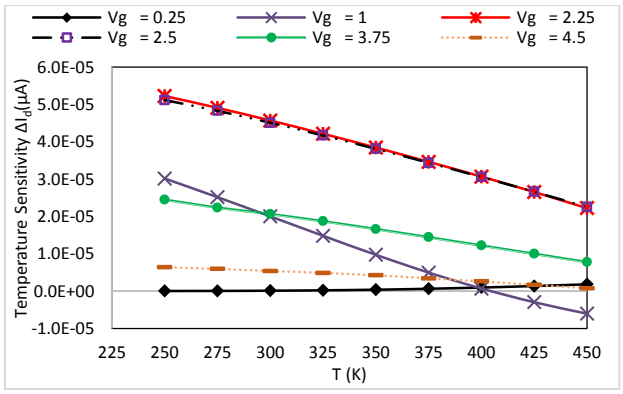

Figure 4. Temperature characteristics of SiNWT at Lg = 85 nm

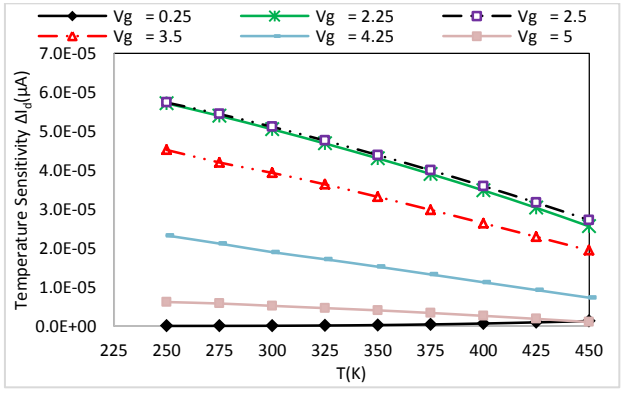

Figure 5. Temperature characteristics of SiNWT at Lg = 105 nm

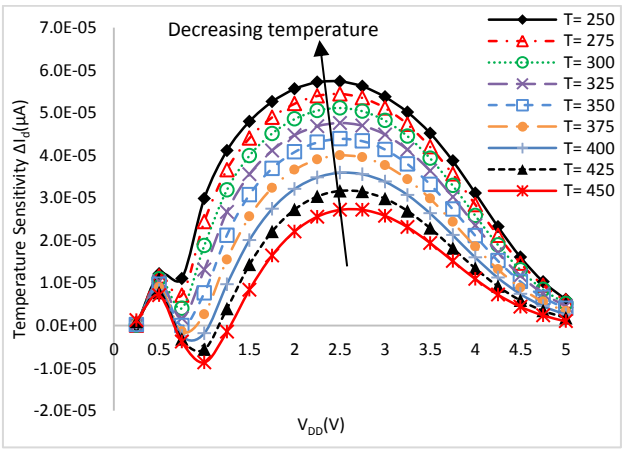

Figure 6. ΔI_d-V_{DD} characteristics of SiNWT at Lg = 105nm

B. *GeNWT Performance*

In the second scenario, GeNWT was considered. The impact of changing channel length on the temperature and electrical characteristics of GeNWT was investigated and compared with the obtained results from the first scenario of SiNWT. Hence, Figure 7 to Figure 11 present the temperature sensitivity values depending on operating voltages and surrounding temperature. Only six of twenty-one operating voltages are illustrated in the figures to increase clarity. It is obvious that the temperature sensitivity decreases with increasing ambient temperature and varies with changing channel length. The highest values of temperature sensitivity as a function of drain current variation were obtained at V_{DD} = 0.75 V for Lg = 25 nm; followed by max ΔId at V_{DD} = 1.5 V for Lg = 45 nm, V_{DD} = 2 V for Lg = 65 nm, V_{DD} = 2.25 V for Lg = 85 nm, and finally V_{DD} = 2.5 V for Lg = 105 nm.

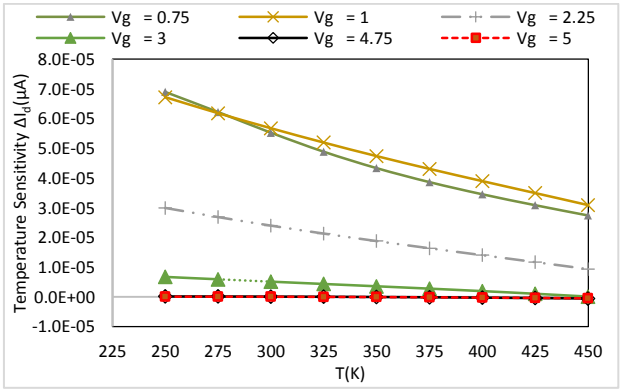

Figure 7. Temperature characteristics of GeNWT at Lg = 25 nm

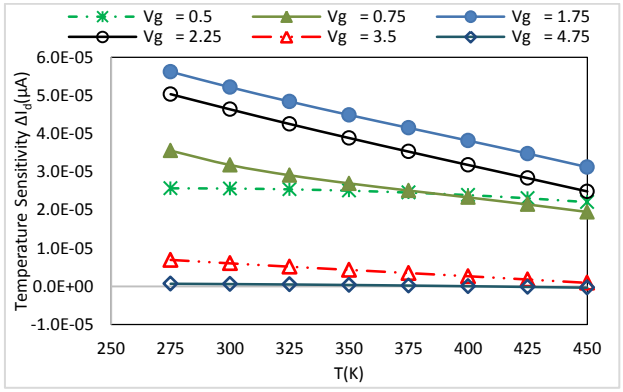

Figure 8. Temperature characteristics of GeNWT at Lg = 45 nm

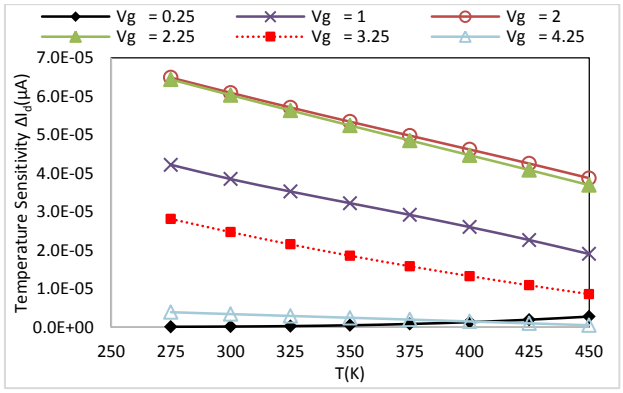

Figure 9. Temperature characteristics of GeNWT at Lg = 65 nm

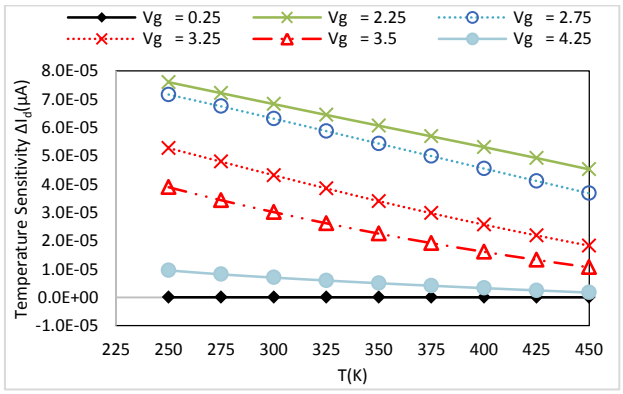

Figure 10. Temperature characteristics of GeNWT at Lg = 85 nm

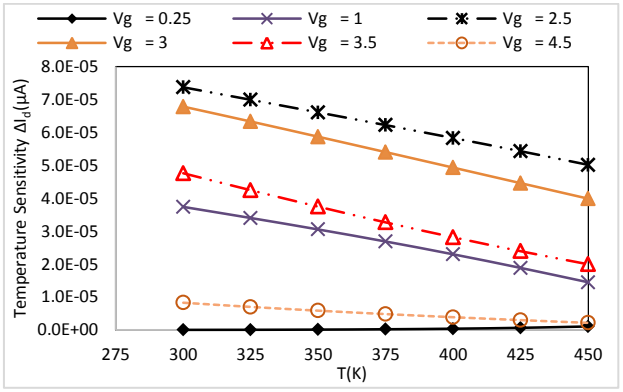

Figure 11. Temperature characteristics of GeNWT at Lg = 105 nm

Figure 12 demonstrates the changes in ΔId with increasing operating voltage, V_{DD} for various ambient temperature at channel length, Lg = 85. This results represent the highest obtained temperature sensitivity for GeNWT. Overall, maximum sensitivities (max ΔId) were observed at lower V_{DD} voltages with short channel lengths (25 to 45 nm) while at longer channel length, the highest sensitivity was achieved with higher values of operating voltages.

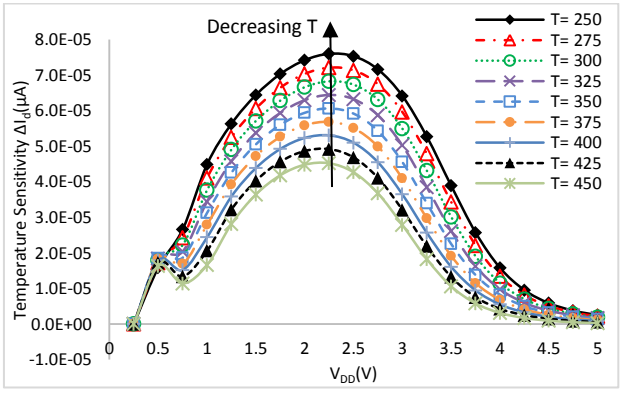

Figure 12. ΔI_d-V_{DD} characteristics of GeNWT at Lg= 85 nm

C. SiNWT and GeNWT Comparison

In terms of temperature characteristics, Fig. 13 compares the optimized operating voltage for SiNWT versus GeNWT based on the best temperature sensitivity with channel length. The figure is based on the obtained results of temperature sensitivity for both transistors. The displayed optimized operating voltage V_g represent the peaks of temperature sensitivity attained. It is very clear that the temperature sensitivity will increase remarkably by increasing channel length for both of SiNWT and GeNWT as well. Both transistors maintain consistent operating voltages regardless channel length. Only at 45 nm channel length, the optimized operating voltages are different.

In our simulations, three electrical characteristics were evaluated depending on channel length for both SiNWT and GeNWT. Figure 14 depicts subthreshold swing (SS) for SiNWT and GeNWT. SS value is an important indicator of transistor switching speed. As fast switching of the transistor is required SS to be as small as possible. As shown in the figure, for the simulated gate length (Lg = 25, 45, 65, 85 and 105 nm) of SiNWT and GeNWT, SiNWT achieved the smallest values of SS and closest to ideal SS value which is approximately ≈ 60 mV/dec at T= 300 K. It is obvious that, the SS value decreases with increasing channel length regardless of semiconductor material. For Lg =105 nm, SS of SiNWT and GeNWT were 61.20 mV/dec and 83.76 mV/dec respectively which is the best obtained values. The worst SS values for both transistors were obtained at the shortest channel length, 45 nm. Those results clarify that the SiNWT outperformed GeNWT and scored the best SS vales for the all range of Lg.

Figure 15 shows the characteristics of threshold voltage (V_{th}) for SiNWT versus GeNWT. It is noticeable that V_{th} is proportionally increased with increasing channel length. Generally, higher threshold voltage is an important factor to sustain power proficiency, thus lead to reduce I_{OFF} which is more needed for transistor's best performance and electrical characteristics stability too. For simulated channel length at T= 300 K, SiNWT outperformed GeNWT and achieved the highest values of V_{th} for all channel lengths. The highest V_{th} of SiNWT and GeNWT were occurred at Lg = 105 nm, with values of 0.775 V and 0.590 V respectively. On the other hands, the lowest threshold voltages were occurred at the shortest channel length of Lg = 25 nm and equal to 0.432 V and 0.249 V for SiNWT and GeNWT respectively. Drain induced barrier lowering (DIBL) for SiNWT versus GeNWT is compared in Figure 16. Here it is better to mention that lower values of DIBL are needed. It can be seen that as long as increasing channel length (Lg), DIBL decreased and SiNWT values are slightly less than GeNWT values.

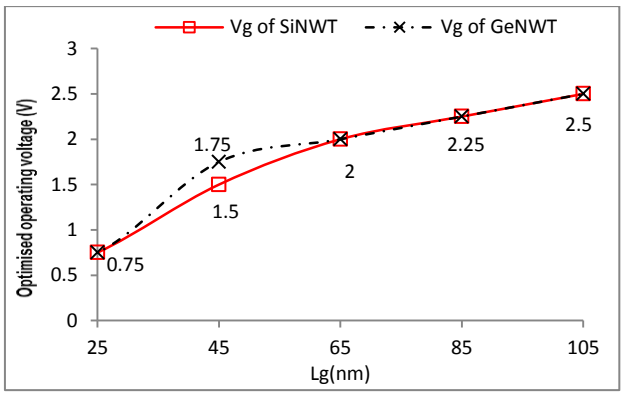

Figure 13. Optimized operating voltage Vs. channel lengths based on best temperature sensitivity for SiNWT and GeNWT

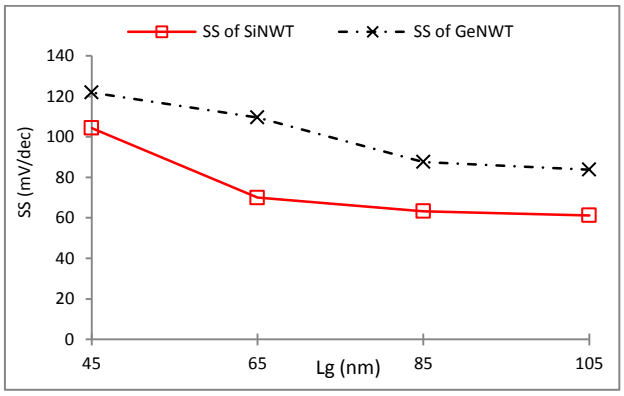

Figure 14. Subthreshold Swing for SiNWT and GeNWT for varying channel length at T = 300 K

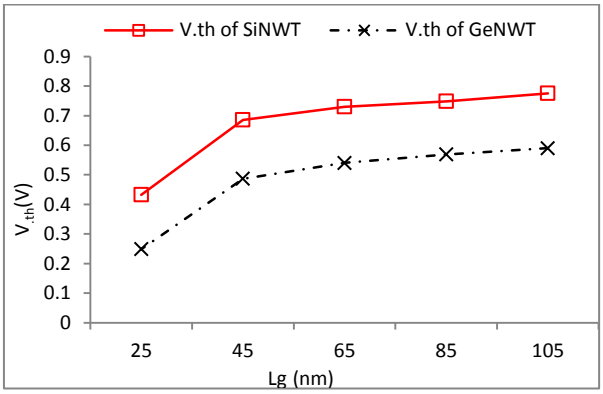

Figure 15. Threshold voltage of SiNWT Vs GeNWT for varying channel length at T = 300 K

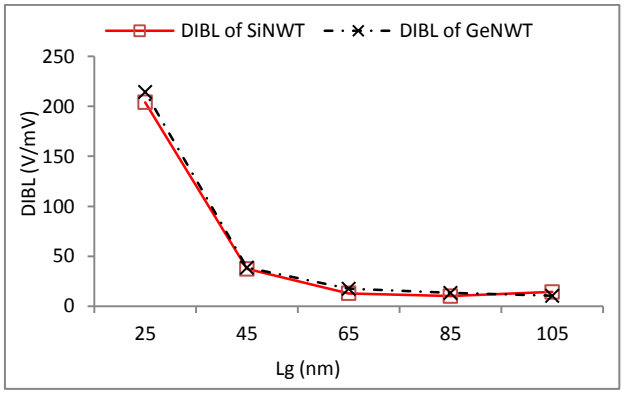

Figure 16. DIBL of SiNWT Vs GeNWT for varying channel length at T = 300 K

5. Conclusions and Future Works

The effects of changing Lg on SiNWT and GeNWT temperature and electrical characteristics were investigated. The obtained results show that with diode mode transistor connection, the best increments –sensitivity- in current (ΔI_d) with temperature occurred between 25 nm to 85 nm channel length range, and beyond will be stable without any effect by

increasing Lg, while for GeNWT, it always increased with increasing Lg. For the electrical parameters based on (SS, Vth and DIBL), the SiNWT shows better electrical characteristics than the GeNWT for all ranges of Lg.

In this paper, only one dimension of channel which is channel length was considered in our comparison. For future work, other dimensions including channel diameter and oxide thickness will be investigated. The application of NWT as temperature sensor was the main concern of this study. However, a huge variety of NWT applications especially in biomedical field will be interested.

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