# Performance Analysis of Quantum Dot Cellular Automata (QCA) based Linear Feedback Shift Register (LFSR) 

Birinderjit Singh Kalyan*1 and Balwinder Singh ${ }^{2}$<br>${ }^{1}$ I K Gujral Punjab Technical University, Jalandhar, India<br>${ }^{2}$ ACS Division, Centre for Development of Advanced Computing (C-DAC), Mohali, India (Ministry of Electronics and Information Technology, Govt of India)

Received 12 Feb. 2019, Revised 28 Feb. 2020, Accepted 4 Mar. 2020, Published 1 May 2020


#### Abstract

The latest trends in the digital design circuits are based on Quantum Dot based structures. The Quantum-dot Cellular automata is paradigm in the area of Nano chip design in terms of their size and low power, which plays a significant role in the Nano electronic industry. This paper presents a novel robust design of LFSR which consumes lesser power than conventional design which is restructured using QCA based XOR gate and D Flip Flop. The simulation of the proposed design were done using coherence engine vector of QCA designer tool. The D flip flop show $41 \%$ lesser complexity and power with the single latency. The XOR Gate is designed with 22 QCA Cells and complexity of $0.02 \mu \mathrm{~m}^{2}$ and latency of 0.75 cycles as compare to previous design which was having 28 cells. The proposed 4 Bit LFSR is designed using four D flip flops and one XOR gate, further average power dissipation is calculated.


Keywords: Quantum Cellular Automata (QCA), Majority Logic, Linear Feedback Shift Register (LFSR), Combinational Logic, QCA Designer, Flip Flop (FF), Clock (Clk).

## 1. InTRODUCTION

With continuous scaling of feature size, as suggested by Gordon Moore, the transistor density is increased by past few decades. The high density leads to increase in heat generated per switching cycle. The latest developments for heat dissipation are not effective which harms the chip very tremendously [1]. Another factor that affects the working of nano scaled devices is the scaling down of transistor which leads to voltage and current leakages. These problems may be resolved with the introduction of latest technologies in the manufacturing industry and designer to introduced low powered circuits. Still the research has been carried out which might either replace or augment the conventional CMOS technology as nano scale devices crosses its physical limits to its maximum extent. The future of the Nano scaled devices is quantum dots which works on the principle of mutual interaction between the cells and magnetism.

## 2. QCA REVIEW

The QCA stores logic states not as voltage levels but based on the position of individual electrons [2] shown in Figure 1(a). The QCA cell contains four quantum-dots that are located at the corners of a square. There are two
additional mobile electrons for a cell which are allowed to tunnel among neighboring sites. The columbic repulsion which exists between two electrons forces them to relocate its position in opposite corners which arises the concept of polarization. Consequently, there are only two stable states for representing the binary information " 1 " and " 0 ". When polarization is " -1 ", the logic become " 0 " and when the polarization is " +1 ", the logic is said to be " 1 ". The QCA standard wire can be simply constructed by cascading a chain of QCA cells as illustrated in Figure 1(b).


Figure 1 (a). Schematics of binary QCA cells
Figure 1(b). Schematics of a QCA wire


## 3. QCA MAJORITY GATE

The basic elements of QCA are designed with the combination of various logic gates. These logic gates are designed using various binary majority decisions elements. The evaluation is done using boolean expressions for multiple gates and hence the majority gate is thus come into existence. The Inverter or NOT gate is designed as shown in Figure 2(a), in which two opposite polarized are place diagonally to each other; the resulted output is inverse of the input. The Three-input majority gate is implemented by using five QCA cells set shown in Figure 2(b), the input cells are designated with A, B, and C and cell M is the output cell which depends upon the polarization of the various cells present. The logic expression of the 3 -input majority gate is expressed by Eq. 1.
$\mathrm{M}(\mathrm{A}, \mathrm{B}, \mathrm{C})=\mathrm{AB}+\mathrm{BC}+\mathrm{AC}$

The five input majority gate is also designed by placing the cells as shown in Figure 2(c), this innovative idea was introduced by Rahimi Azghadi et al [6] which optimized Boolean expression. In this A, B, C, D, E act as input of the five input majority gate and output is designated with M . The output from majority gate depends upon the various polarizations of ten cells in the majority gate. The five input majority gate whose logic function is expressed by Eq. 2.

$$
\begin{align*}
& \mathrm{M}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D}, \mathrm{E})=\mathrm{ABC}+\mathrm{ABD}+\mathrm{ABE}+\mathrm{ACD}+\mathrm{ACE}+ \\
& \mathrm{ADE}+\mathrm{BCD}+\mathrm{BCE}+\mathrm{BDE}+\mathrm{CDE} \tag{2}
\end{align*}
$$



Figure 2(a). QCA Inverter


Figure 2(b). QCA 3 Input majority gate



Figure 2(c). QCA 5 input majority gate

The clock signals in various digital circuits are main elements which synchronized the digital circuits and control the data flow in QCA circuits. In QCA clocking sequence, there are four different successive phases categorized into four clock zones and 90 degree phase delay exists in between the subsequent clock zones as shown in Figure 3. These four clock phases are: Switch, Hold, Release and Relax. As discussed in [4], the noise is much more concern in three input majority gate structure, thereby different clock zone are positioned at the input cells, middle QCA cells and output of the majority gate.


Figure 3. Clocking Mechanism in QCA

## 4. QCA BASED D FLIP FLOP

The logic diagram of D Flip Flop is shown in Figure 4. In this design, D input is fed directly to the input gate and another complement of D is fed to the other NAND gate with a clock signal. The resultant Q and its complement of Q that is $\mathrm{Q}(\mathrm{t}+1)$ is illustrated in Table 1. As described in characteristics table, if $D$ is switched to logic 1 then output state will switch to set state and if D is at logic 0 then output will have logic zero. It shows that the next state of the D flip flop doesn't depend upon present state Q and $\mathrm{Q}(\mathrm{t}+1)$ is equal to the input D .


Figure 4. Logic diagram of D Flip Flop

TABLE I. TABLE TRUTH TABLE/ DESIGN VECTOR OF D FLIP FLOP

| CLK |  | D | OUT 'Q' |
| :---: | :---: | :---: | :---: |
| 0 |  | 0 | 0 |
| 0 | 1 |  | 0 |
| 1 | 0 | 0 |  |
| 1 | 1 | 1 |  |
| 0 | 0 | 0 |  |
| 0 | 1 | 0 |  |
| 1 | 0 | 0 |  |
| 1 | 1 | 1 |  |

When the clock (clk) pulse as input is enabled the data present at the input of the D flip flop is transferred to the ' Q ' output. The D flip flop is designed using five majority gates as shown in Figure 5. This design is having one inverter gate which is fed to majority gate along with original D Flip flop. The output is feedback to one of the input of the five input majority gate.


Figure 5. D Flip Flop Using Majority Gate


Figure 6. Proposed D Flip Flop
D flip flop is implemented using QCA designer as shown in Figure 6. The QCA implementation requires 20 cells, with an area of $0.02 \mu \mathrm{~m} 2$ which is having $58.3 \%$ less complexity then previous design and area utilization is $50 \%$ less than the conventional design. The four clock zone are used for designing the D Flip Flop, hence the
latency is 1. The simulation results represented in Figure 7 shows the consistent clock cycle denote with 'clk' and input denoted as 'D' whose vectors as shown in Table 1, the output is denoted with 'out'. The output is reflected at the output after the delay of 1 clock cycle hence the latency is 1 . The performance analysis of D flip flop and other flip flops are described in Table 2, comparison with the best previous structure and proposed design.


Figure 7. Simulation Results of D Flip Flop

TABLE II. : PERFORMANCE ANALYSES OF FLIP FLOPS

|  | Previous Design |  |  | Proposed Design |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & F \\ & F \end{aligned}$ | Compl exity | Are <br> a(n <br> m) | Total Area (nm2) | Co <br> mpl <br> exit <br> y | Ar <br> ea( <br> nm <br> ) | $\begin{gathered} \mathrm{To} \\ \mathrm{tal} \\ \mathrm{Ar} \\ \mathrm{ea} \\ (\mu \\ \mathrm{m} 2 \\ ) \\ \hline \end{gathered}$ | Lat enc y | Quant <br> um <br> Cost <br> (Late <br> ncy) 2 <br> X <br> Area |
| D | 48[10] | $\begin{gathered} 218 \\ \mathrm{x} \\ 218 \end{gathered}$ | 47524 | 20 | 19 5 x 12 1 | $\begin{gathered} 0.0 \\ 2 \end{gathered}$ | 1 | 0.02 |

## 5. QCA BASED XOR GATE

The QCA based Exclusive-OR gate is designed using one 5 input majority gate and one 3 input majority gate. The gate is having two inputs A and B and the output from the Boolean expression $A+B$ as shown in Table 3. In three input majority gate input A and B is belong along with +1 signal and in five majority gate inversion of input A and B is fed along with output from three majority gate and zero signal as shown in Figure 8.


Figure 8. Design of XOR Gate using Majority Gate

TABLE III. Truth Table/ Design Vector of XOR gate

| A | B | Out |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The QCA based XOR gate as described[7] which was having 28 QCA Cells and complexity of $0.02 \mu \mathrm{~m} 2$ and latency of 0.75 cycle. The proposed design of XOR as shown in Figure 9(a) having 22 cells and complexity of $0.02 \mu \mathrm{~m} 2$ and latency of 0.75 cycle. The XOR gate proposed having 22 QCA cells as compare to 28 cells which was previously design in 2016[7]. The simulation of XOR gate shows the transient response with respect to input A and B with the latency 0.75 whose truth table/design vector are described in Table 3.


Figure 9 (a). QCA Based XOR Gate


Figure 9 (b). Simulation Results of XOR Gate

## 6. PROPOSED LFSR

Linear Feedback Shift Register consists of series connection of flip flops where output of one flip flop is the input of the next flip flop. It is formed by combining XOR gates in the feedback of series of flip flops as shown in Fig 10. The QCA based LFSR is designed using D Flip Flop and XOR gate in Figure 6 and Figure 9 (a). The QCA based LFSR is having 184 QCA cells and utilizes the area of $0.18 \mu \mathrm{~m} 2$ as shown in Figure 11. The simulation results described in Figure 12, the resultant output which is simulated under the Coherence Vector Simulation Engine [8] environment described in Table 4 and the design vector
which are used for simulation of the design in QCA designer tool are in Table 5. The simulation results of LFSR is given in Figure 12, the response reflected at the output after the delay of one clock cycle with a latency 1. In QCA designer tool 'clk' and 'D' acts as inputs clock and input ' D ', the four clock cycle phases acts as switch, hold, release and relax simulated using coherence vector simulation engine. The relaxation time and total simulation time for the design is $1 . \mathrm{e}-015 \mathrm{sec}$ and $7.0 \mathrm{e}-011$ sec.

TABLE IV. Coherence Vector Simulation Engines [8]

| Parameters | Values |
| :---: | :---: |
| Temperature | 1 Kelvin |
| Relaxation Time | $1.0 \mathrm{e}-015 \mathrm{Sec}$ |
| Time Step | $1.0 \mathrm{e}-016 \mathrm{Sec}$ |
| Total Simulation Time | $7.0 \mathrm{e}-011 \mathrm{Sec}$ |
| Clock High | $9.8 \mathrm{e}-022 \mathrm{~J}$ |
| Clock Low | $3.8 \mathrm{e}-023 \mathrm{~J}$ |
| Clock Shift | $0.00 \mathrm{e}+000$ |
| Clock Amplitude Factor | 2.0 |
| Radius of Effect | 80.00 nm |
| Relative Permittivity | 12.90 |
| Layer Separation | 11.5 nm |



Figure 10. Schematic of LFSR
TABLE V. DESIGN VECTOR OF LFSR

| D | Clk |
| :---: | :---: |
| 1 | 0 |
| 0 | 0 |
| 1 | 1 |
| 0 | 1 |
| 1 | 0 |
| 0 | 0 |
| 1 | 1 |
| 0 | 1 |



Figure 11. QCA based Linear Feedback Shift Register


Figure 12. Simulation Result of LFSR
The Hamiltonian matrix is used to calculate total energy and power in a array of QCA Cells. Hence energy dissipation of a QCA cell in one clock cycle TCC $=[-\mathrm{T}, \mathrm{T}]$ is derived in respect to Hamiltonian and coherence vectors as described in equation 3.
$E_{d i s s}=\frac{\hbar}{2} \int_{-T}^{T} \vec{\Gamma} \cdot \frac{d \vec{\lambda}}{d t} d t=\frac{\hbar}{2}\left([\vec{\Gamma} \cdot \vec{\lambda}]_{-T}^{T}-\int_{-T}^{T} \vec{\lambda} \cdot \frac{d \vec{\Gamma}}{d t} d t\right)$
This tool estimates the dissipated energy of whole circuit for each input combinations in various tunneling energy levels under non-adiabatic switching [15]. The upper bound power dissipation model [15] is given shown in equation 4.
$P_{\text {diss }}=\frac{E_{\text {diss }}}{T_{c c}}\left\langle\frac{\hbar}{2 T_{c c}} \vec{\Gamma}_{+} \times\left[-\frac{\overrightarrow{\Gamma_{+}}}{\left|\overrightarrow{\Gamma_{+}}\right|} \tanh \left(\frac{\hbar\left|\overrightarrow{\Gamma_{+}}\right|}{k_{b} T}\right)+\frac{\vec{\Gamma}_{-}}{\left|\vec{\Gamma}_{-}\right|} \tanh \left(\frac{\hbar\left|\overrightarrow{\Gamma_{-}}\right|}{k_{b} T}\right)\right]\right.$

TABLE VI. ENERGY DISSIPATION RESULTS

| $\begin{gathered} \text { Desi } \\ \text { gn } \end{gathered}$ | Average Leakage Energy Dissipation (MeV) |  |  | Average Switching Energy Dissipation (MeV) |  |  | Average Energy <br> Dissipation (MeV) |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{aligned} & 0.5 \\ & \text { Ek } \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.0 \\ & \text { Ek } \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.5 \\ & \mathrm{Ek} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 0.5 \\ & \text { Ek } \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 1.0 \\ & \text { Ek } \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.5 \\ & \text { Ek } \\ & \hline \end{aligned}$ | $\begin{gathered} 0.5 \\ \text { Ek } \\ \hline \end{gathered}$ | 1.0 Ek | 1.5 Ek |
| Prev ious DFF Desi gn | $\begin{aligned} & 11 . \\ & 51 \end{aligned}$ | $\begin{aligned} & 31 . \\ & 91 \end{aligned}$ | $\begin{aligned} & 54 . \\ & 69 \end{aligned}$ | $\begin{aligned} & 35 . \\ & 78 \end{aligned}$ | $\begin{aligned} & 30 . \\ & 48 \end{aligned}$ | $\begin{aligned} & 25 . \\ & 66 \end{aligned}$ | $\begin{aligned} & 47 . \\ & 28 \end{aligned}$ | $\begin{aligned} & 62 . \\ & 39 \end{aligned}$ | $\begin{aligned} & 80 . \\ & 34 \end{aligned}$ |
| Prop osed DFF Desi gn | $\begin{gathered} 9.3 \\ 7 \end{gathered}$ | $\begin{gathered} 29 . \\ 7 \end{gathered}$ | $\begin{aligned} & 52 . \\ & 78 \end{aligned}$ | $\begin{aligned} & 40 . \\ & 08 \end{aligned}$ | $\begin{aligned} & 33 . \\ & 73 \end{aligned}$ | $\begin{gathered} 28 . \\ 05 \end{gathered}$ | $\begin{aligned} & 49 . \\ & 81 \end{aligned}$ | $\begin{gathered} 63 . \\ 49 \end{gathered}$ | $\begin{aligned} & 80 . \\ & 83 \end{aligned}$ |
| Prop osed LFS R Desi gn | 12 2.5 1 | $\begin{gathered} 14 \\ 0.9 \\ 1 \end{gathered}$ | $\begin{gathered} 19 \\ 4.6 \\ 9 \end{gathered}$ | $\begin{gathered} 13 \\ 5.7 \\ 8 \end{gathered}$ | $\begin{gathered} 13 \\ 0.4 \\ 8 \end{gathered}$ | $\begin{gathered} 12 \\ 5.6 \\ 6 \end{gathered}$ | $\begin{gathered} 14 \\ 7.2 \\ 8 \end{gathered}$ | 16 2.3 9 | 10 0.3 4 |

## 7. Simulation Results

The Proposed LFSR is having lowest complexity gate in which D Flip Flop and XOR gate are building block having $58.3 \%$ and $50 \%$ lesser complexity then previous best reported designs, hence the lower complexity and low power dissipation of novelty of LFSR proves and suitable for low power devices for complex digital circuits. To verify the proposed D flip flop design with the previous design, the QCA designer version 2.0.3 is used with the coherence vector simulation engine setup [8]. The Table 4 briefly lists the various parameters assumptions values using for the simulation. The value of relative permittivity set as default as 12.9 for the hetero structure based semiconductor. The Figure 7 presents the simulation waveform of proposed D Flip flop design, the output appears after the latency of 1 clock cycle and having the complexity 20 cell which is 41 percent lesser then previous design. The Figure 9(b) represents the simulation waveform of XOR gate which is having the latency of 1 clock cycle, complexity of 32 Cells and covering the area of $0.04 \mu \mathrm{~m}^{2}$. The figure 12 shows the simulations waveform for the LFSR design. The output appears after the latency of 1 clock cycle after the input vector is applied. The Table 6 describes the energy dissipation result of D Flip Flop and LFSR at 0.5 Ek, 1.0 Ek, and 1.5 Ek at 2 Kelvin. The average switching energy dissipation is the transaction from one clock cycle to another clock cycle. The power of the proposed LFSR are also calculated which can be used to design more complex low power Nano scale random pattern generator for Nano communication architectures.


Figure 12. Complexity analyzes of D flip flop


|  | Average Leakage Energy <br> Dissipation (MeV) |  |  | Average Switching Energy <br> Dissipation (MeV) |  |  | Average Energy Dissipation <br> (MeV) |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 0.5 Ek | 1.0 Ek | 1.5 Ek | 0.5 Ek | 1.0 Ek | 1.5 Ek | 0.5 Ek | 1.0 Ek | 1.5 Ek |
| $\square$ Previous DFF Design | 11.51 | 31.9 | 54.69 | 35.78 | 30.48 | 25.66 | 47.28 | 62.39 | 80.34 |
| $■$ Proposed DFF Design | 9.37 | 29.7 | 52.78 | 40.08 | 33.73 | 28.05 | 49.81 | 63.49 | 80.83 |
| $■$ Proposed LFSR Design | 122.51 | 140.91 | 194.69 | 135.78 | 130.48 | 125.66 | 147.28 | 162.39 | 100.34 |

Figure 13. Energy dissipation analyses of D Flip Flop and Proposed LFSR

## 8. CONCLUSION

This paper presents the novel approach of implementing and designing 4 bit LFSR by using four D flip flop and one XOR gate in quantum-dot cellular automata with minimum area, latency, complexity and
energy dissipation as compared to previous design. The proposed D Flip Flop is designed using a five input majority gate and an Inverter which is $58.3 \%$ less complex then other reported designs. The XOR gate design utilizes a three input majority gate, a five input majority gate and two inverter. It uses 22 QCA cells and having latency of
0.75 clock cycle. The proposed novel 4 bit LFSR design utilizes four D flip flop and a XOR gate having the latency 1 clock cycle. Four bit LFSR is having 184 QCA cells and utilizes the area of $0.18 \mu \mathrm{~m}^{2}$. he analysis has been carried out and evaluation on the basis of average leakage energy dissipation, average switching energy dissipation and average energy dissipation.

## References

[1] C. S. Lent; P. D. Tougaw, A device architecture for computing with quantum dots," in Proceeding of the IEEE, vol. 85-4, pp. 541-557, April 1997 [doi: 10.1109/5.573740]
[2] M. Rahimi Azghadi, O. Kavehei, K. Navi, A Novel Design for Quantum-dot Cellular Automata Cells and Full Adders, Journal of Applied Sciences 7 (2007) 3460-3468.
[3] W. Liu, E. E. Swartzlander Jr, M. O'Neill, Design of Semiconductor QCA Systems, Artech House, 2013.
[4] A. P. Chandrakasan and R. W. Brodersen, "Minimizing power consumption in digital CMOS circuits," in Proceedings of the IEEE, vol. 83, no. 4, pp. 498-523,Apr1995.
[5] Balwinder Singh and Arun Khosla "Power Optimization of Linear Feedback Shift Register (LFSR) for Low Power BIST" IEEE International Advance Computing Conference (IACC 2009) Pages: 311-314, 2009
[6] Atul Kumar Nishad, Rajeevan Chandel "Analysis of Low Power High Performance XOR Gate Using GDI Technique" International Conference on Computational Intelligence and Communication Networks, pp.187-191, 2011.
[7] Gurmohan Singh, R. K. Sarin, Balwinder Raj "A novel robust exclusive-OR function implementation in QCA nanotechnology with energy dissipation analysis" Journal of Computational Electronics Volume 15 Issue 2, June 2016 Pages 455-465. [doi: 10.1007/s10825-016-0804-7]
[8] QCA Designer Tool Version 2.0.3; http://www.mina.ubc.ca/qcadesigner_downloads
[9] Craig. S. Lent, P. Douglas Tougaw, and Wolfgang Porod, "Quantum cellular automata: the physics of computing with arrays of quantum dot molecules" In: Proceedings of the workshop on physics and computing, pp.5-13 (1994) [doi: 10.1109/PHYCMP.1994.363705]
[10] Sara Hashemi, Keivan Navi, "New robust QCA D flip flop and memory structures" Microelectronics Journal 929-940, 2012. [doi: 10.1016/j.mejo.2012.10.007]
[11] Mohammad Torabi "A New Architecture for T Flip Flop using Quantum-Dot Cellular Automata" IEEE 3rd Asia Symposium on Quality Electronic Design, 2011.[doi: 10.1109/ASQED.2011.6111764]
[12] J. Huang, M. Momenzadeh, F. Lombardi, "Design of sequential circuits by quantum-dot cellular automata", Microelectronic Journal 38 (2007) 525-537. [doi: 10.1016/j.mejo.2007.03.013]
[13] Kun Kong, Yun Shang and Ruqian Lu, "Counter Designs in Quantum-Dot Cellular Automata" 10th IEEE International Conference, Aug 17-20, Korea 2010. [doi: 10.1109/NANO.2010.5698033]
[14] Mohammad Torabi "A New Architecture for T Flip Flop using Quantum-Dot Cellular Automata" IEEE 3rd Asia Symposium on Quality Electronic Design, 2011.[doi: 10.1109/ASQED.2011.6111764]
[15] S. Srivastava; S. Sarkar; S. Bhanja, "Power Dissipation Bounds and Models for Quantum-dot Cellular Automata Circuits"., IEEE Conference on Nanotechnology, vol. 1, pp. 375.378, June 2006. [doi: 10.1109/NANO.2006.247655]
[16] Bahar, A.N., Uddin, M.S., Abdullah-Al-Shafi, M., Bhuiyan, M.M.R. and Ahmed, K., 2018. Designing efficient QCA even parity generator circuits with power dissipation analysis. Alexandria engineering journal, 57(4), pp.2475-2484.[doi: https://doi.org/10.1016/j.aej.2017.02.002]
[17] Mohammadi, M., Mohammadi, M. and Gorgin, S., 2016. An efficient design of full adder in quantum-dot cellular automata (QCA) technology. Microelectronics journal, 50, pp.35-43.[ https://doi.org/10.1016/j.mejo.2016.02.004]
[18] Zhang, Rumi, Konrad Walus, Wei Wang, and Graham A. Jullien. "Performance comparison of quantum-dot cellular automata adders." In 2005 IEEE International Symposium on Circuits and Systems, pp. 2522-2526. IEEE, 2005.[ 10.1109/ISCAS.2005.1465139]
[19] Adelnia, Yaser, and Abdalhossein Rezai. "A Novel Adder Circuit Design in Quantum-Dot Cellular Automata Technology." International Journal of Theoretical Physics 58, no. 1 (2019): 184200.[doi: https://doi.org/10.1007/s10773-018-3922-0]
[20] Kalyan B S , Singh Balwinder," Quantum Dot Cellular Automata (QCA) based 4-Bit Shift Register using efficient JK Flip Flop" International Journal of Pure and Applied Mathematics, Volume 118 No. 19 2018, 143-157.


Balwinder Singh, Masters from Panjab University, Doctorate GNDU Amritsar. Research area Low power VLSI Design, Sensor MEMS design and modeling and AI. Published more than 100 research paper in reputed journals and conferences. Presently Joint Director, ACSD and Principal Engineer at ACS Division, Centre for Development of Advanced Computing (C-DAC), Mohali, India.


Birinderjit Singh Kalyan, Masters form Panjab University. Research area is QCA circuit design and low power VLSI design. Published more than 30 research paper in reputed journals and conferences.

