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Low Power Implementation of FIR Filter for De-Noising the EOG Signal

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Abstract: In this paper, we propose a modified FIR filter using canonical signed digit representation and compressor techniques for de-noising the Electrooculography signal (EOG). A dipole, formed between cornea and retina in an eye, resulting in voltage difference with occurrence of eye movement, which in turn generates an electrical signal. These electrical signals, called Electrooculography (EOG) signal and are useful in many medical and bioelectrical applications. To remove the noise in EOG signal an enhanced 16-bit FIR filter is used. The proposed FIR architecture uses canonical signed digit based multipliers and 3:2 or 4:2 compressors to achieve greater improvement in power and delay compared to conventional shift-add method of multiplication. Canonic signed digit (CSD) is used in order to reduce the design complexity of the multiplication by representing the filter coefficients in CSD format. Instead of using Carry Look Ahead adders, 4:2 compressors are used. The proposed approach is implemented on FPGA development kit.

Keywords: Electro-oculography, Canonic Signed Digit, Compressors, FPGA

1. INTRODUCTION

Electrooculography (EOG) is one of the bio-signals that can be measured and monitored. It is a technique for measuring the cornea-retinal standing potential that exists between the front and the back of the human eye. The resulting signal is Electrooculogram. The EOG signal provides the corresponding voltage generated by the eye movement. These measurements are used to study the eye movement pattern and related aspects [1]. Amplitude of this signal ranges between 50-3500 µV and its frequency component ranges from 5-30Hz [2]. Main applications of EOG signals are in ophthalmological diagnosis, recording eye movement and in many Human Computer Interface. EOG has wide range of applications in medical diagnosis, study of different eye movements and Human Machine Interface (HMI). Many noise suppressions techniques for EOG signals have been implemented; out of them band pass FIR filter has accuracy and best processing speed [3]. Multipliers are important and building blocks in Digital Signal Processing, Digital Image Processing.[4] Hence to reduce the complexity in multiplication and to reduce path delays, area of the existing conventional methods, CSD based representation is very effective [5]. CSD representation will be useful for many design-implementation of digital filters and CSD based filter architecture for image conversion [6].

This paper describes the denoising of EOG signal using FIR filtering techniques. Section 2 describes the FIR filter basics. Section 3 focuses on conventional method of multiplication. Proposed method and its implementation in FPGA along with Software/Hardware co-simulation is discussed in sections 4 and 5. Synthesis Results of proposed architectures are mentioned in sections 6. Conclusion is discussed in last section.

2. FIR FILTER

Digital filter is one of the most important block in DSP processing. It has many applications like noise reduction and suppression of unwanted signals. As it resolves to zero in finite time, hence it has an impulse response of finite duration. The equation of FIR filter is as shown below,[7]

$$Y(n) = \sum_{k=0}^{N-1} h(k) * x(n-k) \qquad (1)$$

Where x (n) is input sample, Y (n) is output sample, h (k) is filter coefficient, and N is filter order. Eq. (1) represents FIR filter of order N. The term x (n-k) in (1)

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represents the input to multiplication process with some delay, which is called as taps. These define the filter order in different forms of FIR structures. Basic FIR filter with transposed form is shown in Fig.1. FIR filter Transpose form is having more advantages than direct form [8]. The major building blocks of FIR filter are multiplier, adders and delays. Here multipliers should be fast enough so that overall throughput should not suffer. Multiplication blocks uses adders in combination and delays are used to store sample value in memory for one sample clock cycle. Filter coefficients are obtained by MATLAB FDA tool by designing the 16-bit low pass Equiripple FIR filter with frequency range of 5-30Hz. The obtained filter coefficients are [-192, -288, -352, 224, 864, 1696, 2624, 3552, 4256, 4640]. The designed filter is of 24-order, hence we get 24 filter coefficients in which 12 are mentioned above [h0-h11], remaining coefficients are symmetric in nature.

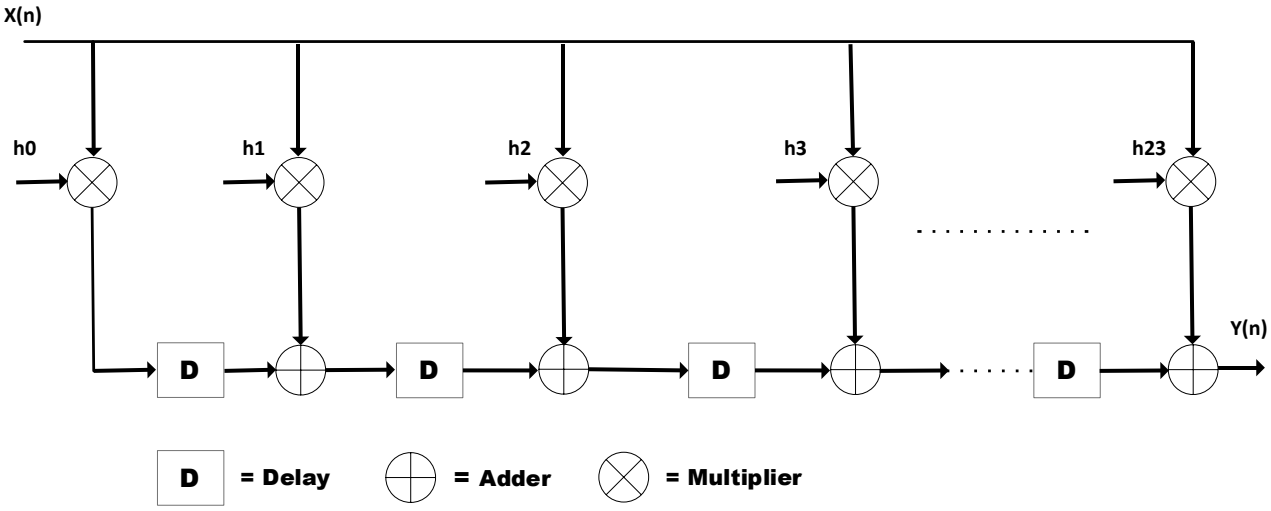

Figure 1. FIR Filter Architecture

3. CONVENTIONAL SHIFT-ADD MULTIPLIER

From the literature survey, it is found that in FIR filter, optimization can be done in multiplier block. Shift and add is a method for implementing binary multiplication. Here, the multiplication with the 0 bits is neglected hence number of commutations are reduced, hence number of logic devices will be reduced which in turn reduces their switching activities, which in turn impacts in reduction of the area and power [9]. Left shifting a binary number by n-bit is equivalent to multiplying the number by 2^n. Shift-Add multiplication on each coefficient is performed by simply shifting the binary number by obtained shift values and adding all the results by using a Ripple Carry Adder (RCA). Filter coefficient 3552 (i.e., h9 and h14) has maximum path delay, hence representing the coefficient in binary form as: 0000 1101 1110 0000, which can be represented as follows: $2^{11} + 2^{10} + 2^8 + 2^7 + 2^6 + 2^5$. Shift-and-Add multiplication has performed instead of a simple binary multiplication. Maximum number of RCAs required for this implementation is for the coefficient h9 and required adders are 5. Maximum delay is shown in Fig.2.

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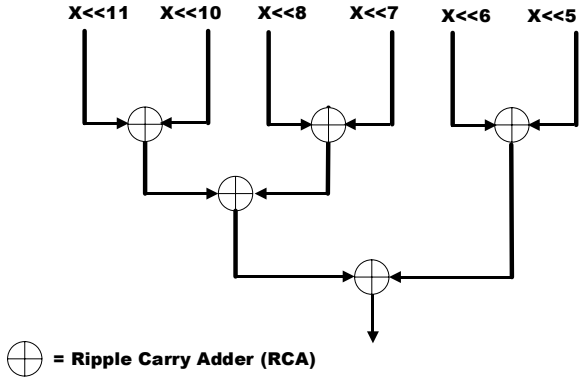

Figure 2. Shift-Add representation for maximum path delay coefficient in Filter

4. FIR FILTER WITH PROPOSED MULTIPLIER

To further optimize filter area and delay, in Shift and add technique the binary number, of filter coefficients represented in CSD form, as it is more efficient than binary representation. CSD is a representation in which number of non-zero terms becomes minimal. It uses ternary number system with digit set of (−1, 0, 1) instead of binary digit set (0, 1). The extra digit "−1", denoted as "1 bar" [10]. In CSD representation, two consecutive non-zero digits are not allowed, which means that 11 or -11 are invalid. There are minimum non-zero binary

elements in CSD representation, which results in reduced number of adders. Therefore, CSD representation implementation in hardware is more efficient, instead of binary representation [11]. Coefficients in CSD are represented as:

$$Y(n) = \sum_{r=0}^{B-1} X_r \, 2^r \qquad (2)$$

Where Xr = 0, 1, -1 (represented as 1 bar)

As Shift-Add, multiplication has 5 RCA, which takes long time for computation, hence to reduce number of RCA filter coefficients are represented in CSD format. For CSD representation, the critical path or the maximum delay for coefficient h7, maximum number of Ripple carry Adders (RCA) required for this is shown in Fig.3. From Fig.2, we get to know that minimum required number of RCAs for multiplication in FIR filter designed using shift-add method is 5 RCA. Where each RCA consists of 1 Half Adder (HA) and N-1 Full Adders (FA) [12]. Minimum required RCAs for CSD based representation is 3 RCA. The proposed multiplier uses less number of RCAs compared to conventional multiplier, and it consumes less area, power and delay than the conventional method.

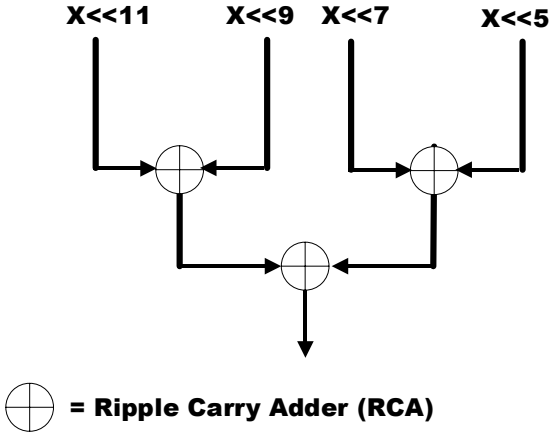

Figure 3. CSD based Representationn for critical path delay coefficients in filter

Instead of using conventional RCA or CSA, ternary adders are proposed for designing an adder block [13]. Instead of using many stages of RCA, in first stage 3 inputs are compressed to two inputs using carry save adder, which are then processed using a normal RCA. The filter coefficients are then converted into CSD format, instead of normal binary representation. Instead of using conventional RCA, which uses more area and higher delay are replaced by a 3:2 or 4:2 compressors [14]. A 3:2 compressor takes 3 inputs and generates 2 outputs as Sum (S) and Carry (C) using XOR gates and MUX as shown in Fig.4. By using this implementation, we get an overall delay of two XOR gates and area is calculated as two XOR gates and one 2:1 MUX. Similarly 4:2 compressor implementation is comprised of two FA (Full Adders), where individual FA are divided into sub-blocks based on XOR gates as discussed in [15]. The optimized compressor design consists of four XOR gates and two 2:1 MUXs is shown in Fig.5. Hence we can observe the overall delay as three times the delay of XOR gates and area is calculated as two 2:1 MUXs and four XOR gates [16]. An RCA is required to add the final S (sum) and C (carry) outputs. FIR Filter with the proposed multiplier architecture is shown in Fig.6

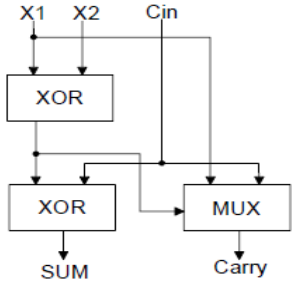

Figure 4. 3:2 Compressor using XOR and MUX gates

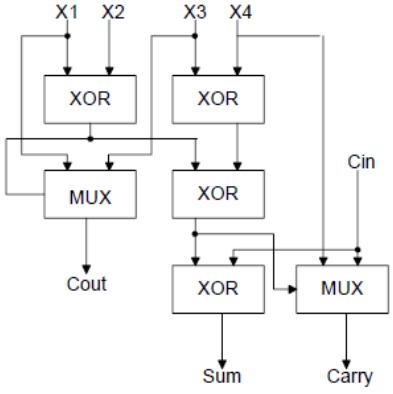

Figure 5. 4:2 Compressor using XOR gates

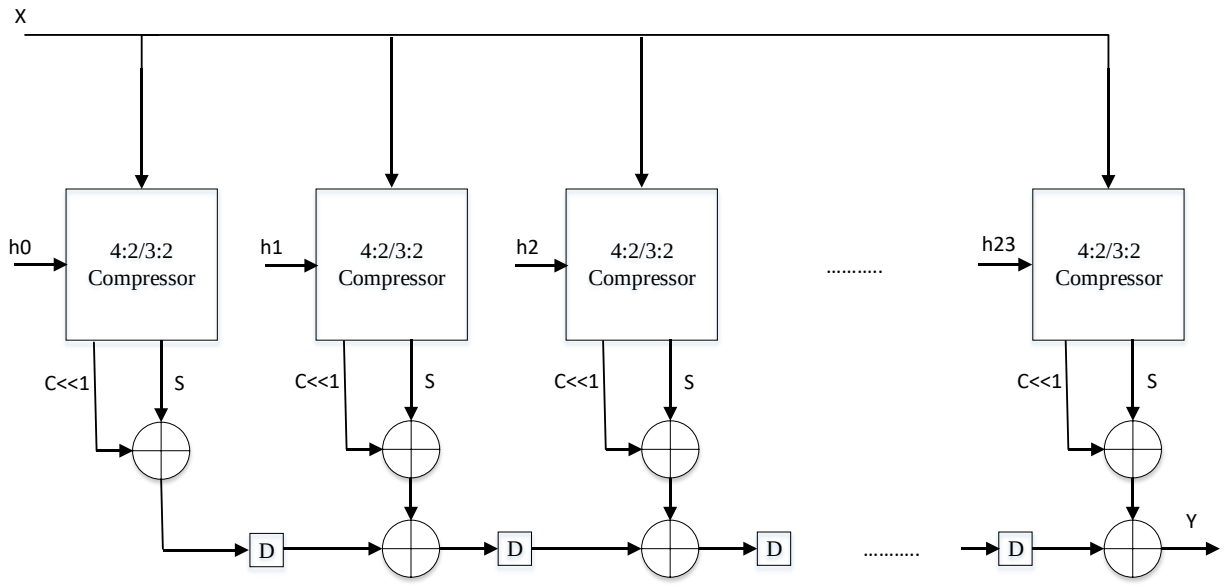

Figure 6. FIR filter using the proposed multiplication architecture

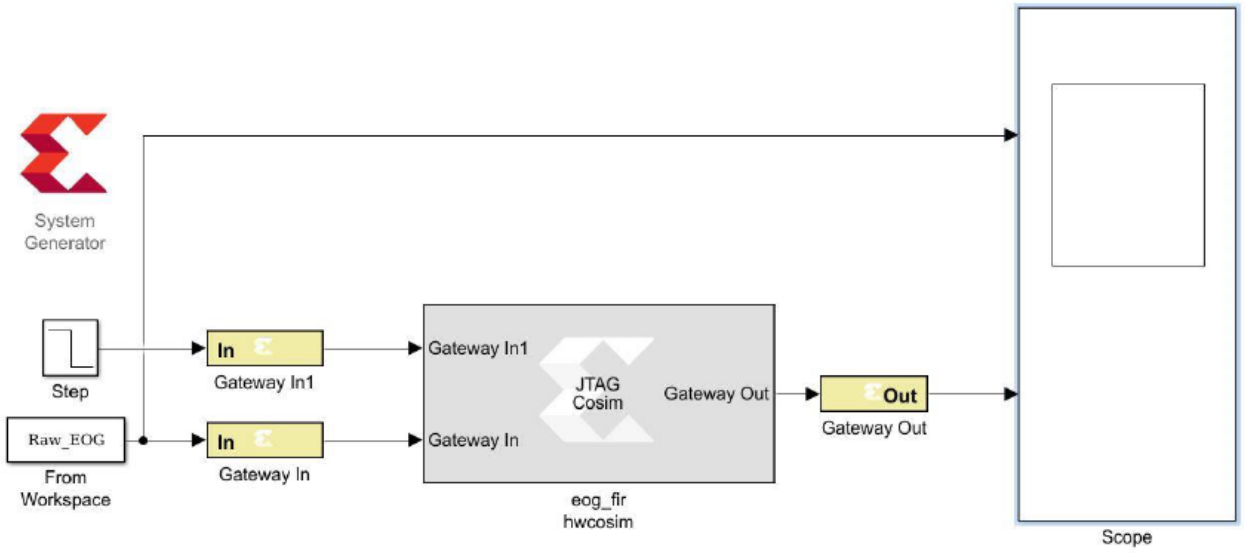

Figure 7. Hardware/Software Co-Simulation Setup For Noise Removal In EOG Signal

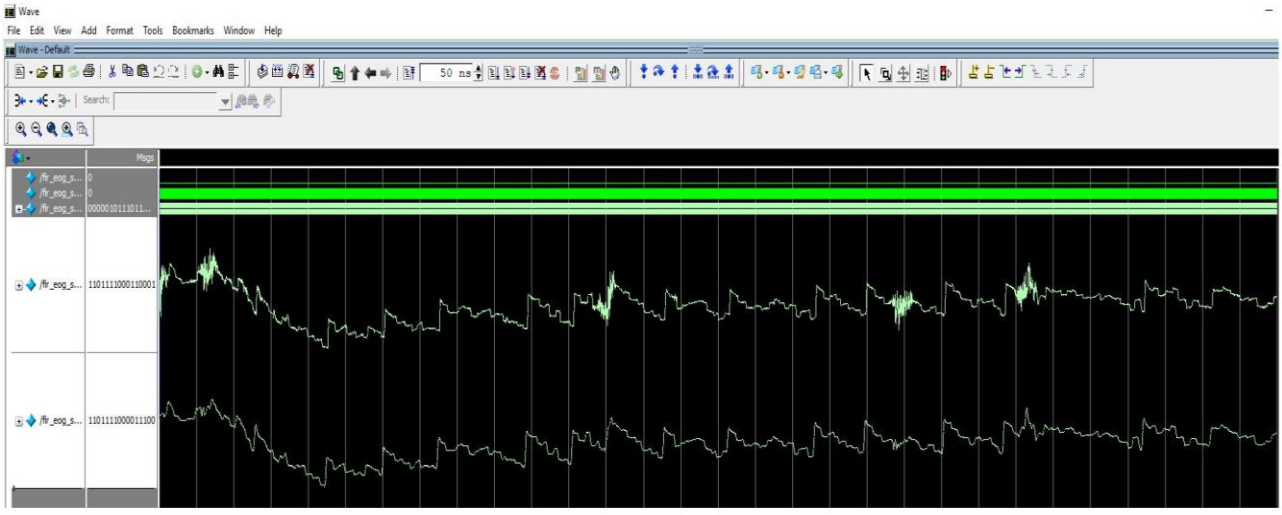

Figure 8. Waveforms of Raw EOG signal and Denoised EOG signal

5. IMPLEMENTATION OF FILTER WITH PROPOSED ARCHITECTURE

The setup for removing noise in EOG signal using proposed method is implemented using Verilog HDL and MATLAB, and hardware/software co-simulation is used. Initially simulation results are verified and then functionality is implemented in hardware/software co-simulation block. In this proposed architecture EOG signal is obtained from [17]. The proposed model is implemented and verified on FPGA Zed Board Zynq evaluation and development kit xc7z020c1g4841 using Xilinx System Generator (XSG) 2016.2. The hardware/software co-simulation setup is shown in Fig.7.

The applied raw EOG signal and its filtered output signal is observed on the scope in XSG. The JTAG co-simulation in XSG generates the Xilinx block set required for the hardware zed board. The output waveform of raw EOG and noise removed EOG signal is shown in Fig.8. The Power Delay Product (PDP) of CSD is increased by 6.73% than the shift-add method and the Power Delay Product of proposed compressor based architecture is increased by 10.24% than the conventional shift-add method.

6. SYNTHESIS RESULTS

In this section, synthesis results of proposed and conventional filter is shown, by comparing their area, power and delays. The results are obtained from cadence 90nm technology design tool. Implementation results of conventional and proposed multipliers is shown in Table 1. Which displays parameters like Delay, Area and Power along with Area Delay Product (ADP), Power Delay Product (PDP), increase in ADP (ADP%), PDP (PDP%), and increase in delay (D%) is also listed in Table 1.

TABLE 1. SYNTHESIS RESULTS OF FIR WITH DIFFERENT MULTIPLICATION TECHNIQUES

Parameter	Shift_Add	CSD	Proposed
Area(μm²)	30795	30009	30491
Power(μW)	5212.67	5031.60	5116.81
Delay(nS)	7.94	7.19	6.51
D(-)%	--	9.45	22.08
PDP	41409.47	36192.31	33295.05
PDP(-)%	--	12.60	19.60
ADP	244635.5	215854.74	198404.9
ADP(-)%	--	11.76	18.90

The proposed architecture has reduced delay compared to conventional methods as shown in Table 1, because of using ternary adders instead of conventional adders. EOG signal can be used to analyze various eye movements such as saccades, fixational movements and vergence. Many eye diseases such as degenerative myopia, retinal disorders, and epileptic nystagmus can be diagnosed. EOG has Drowsiness detection, HMI, and eye-tracking for bio-medical engineering applications.

7. CONCLUSION

In this, we have proposed a modified FIR filter for denoising the EOG signal. In this proposed filter architecture, it uses CSD based representation for minimizing the multiplication and a conventional adders is replaced by 3:2/4:2 compressors. The proposed architecture is compared with the conventional method of shift-add and CSD with RCA and improvements is shown in terms of area, power and delay. The filters have been synthesized and implemented in Zynq development kit

using Vivado Design suit to target the device xc7z020c1g4841. Results show that improvement in PDP, ADP for this filter.

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