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# A Low noise Low power Chopper Stabilized Biopotential Amplifier for Biomedical Applications

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**Abstract:** This paper presents a chopper-stabilized biopotential amplifier designed to amplify ECG and EEG signals. Such amplifier plays an important role in the acquisition of bio-signals in analog front-end of the signal monitoring system. The proposed amplifier is designed with considering primary design goals like power, noise, gain, CMRR, area and offset. To reduce the flicker noise and offset, the chopper stabilization technique is used with OTA. As the parameters like offset, input impedance and 3-dB bandwidth are crucial for monitoring the bio-signals, the chopping frequency for the chopper modulator is carefully selected. Also, due to only one OTA which is the main power consuming block, the overall power dissipation is low. The designed architecture consumes a total power of 8 µW with the gain of 40dB and CMRR of 84 dB. It generates 31nV/ √ Hz with a THD of 13%. The simulations are carried out in Cadence Virtuoso using 180 nm model parameters.

**Keywords:** ECG, Biopotential Amplifier, Sensor, Front-end, Chopper Stabilization, 180nm, Layout

## 1. INTRODUCTION

Bio-signals are generated by the electrochemical activities of specific types of cells which are the parts of the nervous system[1][2]. Electrically, these cells create ground potential but, on the triggering, action potential or potential difference is generated. Table I shows the frequencies and amplitudes of such biopotential signals.

TABLE 1. SPECIFICATIONS OF BIO-MEDICAL SIGNALS [2]

| Signals | Frequency | Amplitude |
|---|---|---|
| ECG | 0.01-200Hz | 1µV-8mV |
| EEG | 0.1-100Hz | 1 µV-250 µV |
| EP | 1Khz-5Khz | 50nV-25 µV |
| EMG | 0.01Hz-10KHz | 60 µV-10mV |

By referring the table I, the biopotential signals have the characteristic of low-frequency small-amplitude which possess strict requirements for the read-out circuit design in terms of power, noise and gain performance. Besides, the presence of the flicker noise in CMOS technology makes the design very challenging [2].

A conventional biopotential monitoring system consists of sensors, drivers, microprocessors, DSP system and radio. The power consumption of each block becomes crucial to minimize the total power dissipation of the system. The overall block diagram of the bio-signal acquisition system using a biopotential amplifier is shown in figure 1.

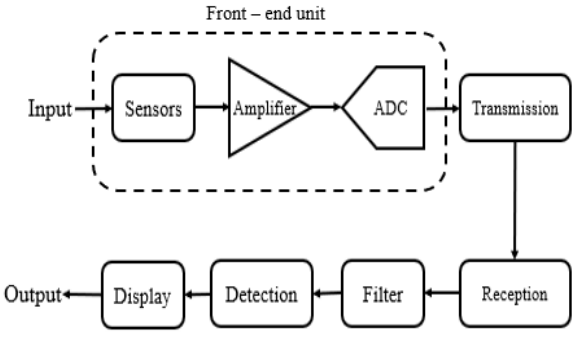


Figure 1. Block diagram of the recording system

The input is generated by the biopotential electrode having a very low amplitude and frequency[3]. Due to this, large gain and good common mode noise rejection

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are required to ensure an accurate diagnosis. Subsequently, the design of the noise reduction method becomes very crucial. Also, the DC offset is generated due to the human body interfaces through the electrodes. So, the offset reduction is essential for such an application. Apart from these issues[4], the input impedance of the biopotential amplifier must be high. To detect the correct signal, sample and hold circuit along with the low pass filter is used. Finally, analog to digital converter (ADC) is used as the final stage to support digital processing for transmission.

This paper represents the AC coupled chopper-stabilized amplifier which employs the integrator at the feedback to create the high pass response of the amplifier and input capacitance to block the DC offset. Also, the noise and power trade-off are addressed and optimize to keep a balance between them. In the following section, various topologies used in the literature for biopotential amplification of ECG and EEG signals are discussed. Finally, proposed architecture with all required analysis and appropriate simulations are discussed with necessary details and the results are compared with the state of art from the literature.

## 2. BIOPOTENTIAL AMPLIFIER

As discussed in the previous section, the biopotential amplifier is a very important block of the analog readout. As it consumes lots of power; it is very much necessary at this point of time to design a biopotential amplifier with good noise and power performance[2].

It can be observed that biopotential amplifier architectures which are available commercially are not fulfilling the specifications of low power applications. For instance, the existing high-performance biopotential amplifier consumes around 130 µW power with 65 $nV/\sqrt{Hz}$, and further, the multi-channel system gives excessive power dissipation considerably reducing battery lifetime[2]. Now let's take a review of some very popular power-efficient biopotential amplifier architectures suitable for the extraction or acquisition of the biopotential signal from the earlier implementations.

The most commonly used biopotential amplifier is three op-amp based topology. Although this topology is ideal for producing high input impedance with high CMRR but has two limitations. First, due to three op-amp, large power dissipation results with poor noise performance results. Also, passive resistors increase noise and area requirements. The alternate topology is using switch capacitor-based architecture. The main benefit here is they are capable to reduce the flicker noise due to working of the capacitor, with reduced input impedance[5], however, the noise fold-over problem occurs which further degrade the overall performance of the said architecture. The third topology is pseudo-resistor-based which performs well in terms of power and noise but requires crucial element matching.

To resolve the above-mentioned issues, the chopper stabilization technique is used to reduce the effect of noise and offset.

### *A. Chopper stabilized biopotential amplifier*

The architecture given in [6] provides good performances in terms of power, noise and common-mode range but use more area due to the additional filtering circuit and due to this, the overall implementation becomes very complex. The next modification is presented in [7] but the noise power and offset are moderate due to missing chopper frequency tuning as compared to its earlier version. So here the authors attempted to combine good design features of all previous implementations to achieve improved performance with simple architecture compared to the reference topology and achieved proper tuning of chopper frequency to improve noise offset and power consumption. The designed architecture succeeded to perform better with lesser complexity as compared to earlier versions but needs additional circuit block for offset cancellation.

Also, in [8] represented a similar kind of architecture but missing optimization for the specifications required for biomedical recording system.

### *B. Chopper stabilization method*

The basic diagram of the chopper stabilization method is shown in figure 2. Apart from the amplifier, it consists of the modulator at input and the demodulator connected to an output of the amplifier.

Here, the modulator and /or demodulator require the clock signal as a carrier signal for the modulation purpose with selected frequency. Also, the flicker noise and thermal noise is considered while designing the amplifier in this work.

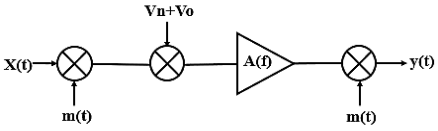


Figure 2. Chopper Amplifier

The clock signal m(t) is applied at one of the inputs of modulator and demodulator, with a frequency $f_{chop}$. Due to the modulation with the high-frequency carrier, the resultant signal or modulated signal shifts at high frequency in the frequency spectrum of the input signal x(t) to the higher frequencies which are the odd harmonics of chopper frequency. Afterwards, the amplifier A(f) amplifies the modulated signal. And then with the same carrier signal, it is demodulated. Due to this, the modulated frequency spectrum shifts to its initial location, and the odd harmonics of chopper

frequency are left. Low pass filter is used to remove the flicker noise which is at a higher location in the frequency spectrum and the offset can be eliminated [6]. There are different topologies available using chopper stabilization method. In the next section, the proposed architecture with chopper stabilization method is discussed

## 3. PROPOSED ARCHITECTURE

Here, the modification is derived by combining the chopper frequency tuning methods used in pseudo-resister-based topology and chopper amplifier uses NMOS version Operational Trans-conductance Amplifier using an additional improved version of Common Mode Feedback block resulting in improved overall performance which is most suitable for biomedical applications. Here, the AC - coupled amplifier is designed to minimize the effect of offset. Also, in feedback R-C network is designed in such a way that it creates a lower cut off frequency of 0.1Hz and OTA has the 3-dB bandwidth of 1KHz. So, the overall amplifier creates a high-pass response which is well suited for such applications.

The block diagram of the proposed architecture is shown in figure 3. The details of each sub-block are described in the following paragraphs.

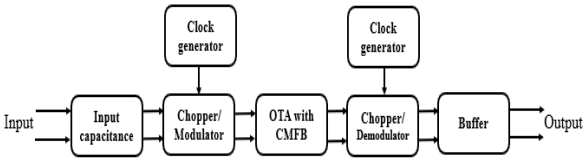


Figure 3. Block diagram of the proposed biopotential amplifier

### A. Clock generator

In figure 4, the gate-level schematic of the clock generator circuit is shown. It consists of the combinational gates like NOT gate and NAND gate. This circuit generates non-overlapping clocks with a 50% duty cycle required to operate the chopper amplifier.

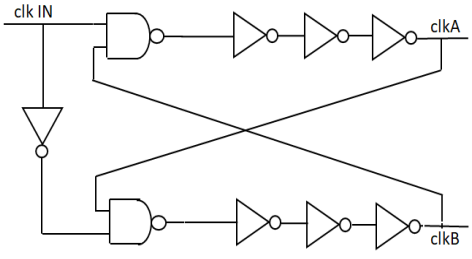


Figure 4. Schematic diagram of the clock generator circuit

### B. Modulator/Demodulator

This block is also known chopper block which helps to reduce the interference of flicker (1/f) noise and DC offset. Here, the Chopper stabilization method is used as discussed in the previous section. Using modulator and demodulator, the flicker (1/f) noise band and DC offsets shift to a higher frequency so that after applying a filter, it can be eliminated [6].

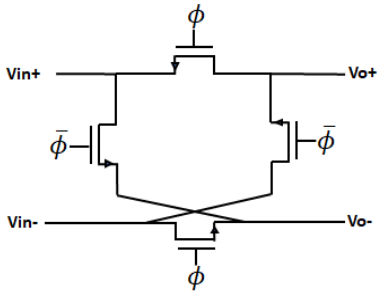


Figure 5. Schematic diagram of the chopper

### C. OTA with CMFB

The CMOS OTA with CMFB is shown in figure 6. As shown in Fig, transistors M1 to M6 are part of the single-stage differential amplifier and transistors M1C to M5C are a part of the CMFB circuit.

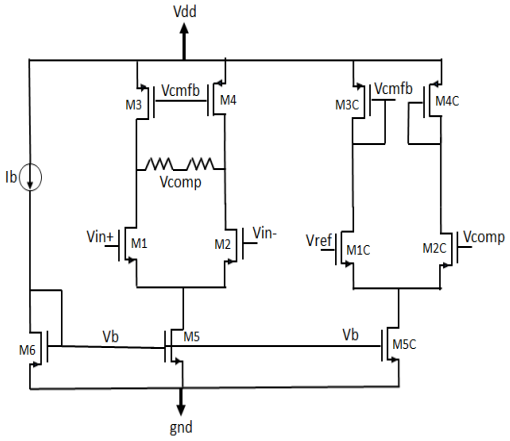


Figure 6. Schematic diagram of OTA with CMFB

To stabilize or maintain the common-mode (CM) level at the output, the common-mode feedback (CMFB) circuit is used in the differential amplifier. It is strongly recommended as even a small difference or mismatch in currents of the two branches, degrades the performance of the impedance at output, and due to large potential difference between the two outputs, the amplifier is in out of balance and thus degrade the performance. Here, the resistive sensing circuit is used to sense the CM output level and provide to feedback network to generate proper biasing current in one of the transistors [7]. Nowadays optimized CMFB circuits are there but, in this work, as per the specification are taken; simple CMFB circuit is used to generate the proper results.

### D. Buffer

In figure 7, the schematic diagram of the two-stage differential amplifier is shown.

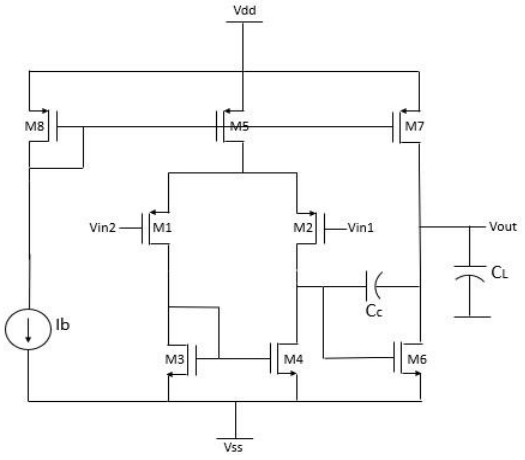


Figure 7. Schematic diagram of a two-stage op-amp

Here, PMOS transistors M1 and M2 are input transistors which are configured as common-source configuration. Transistors M3 and M4 are active loads, and biasing is done with a current mirror by transistors M5 and M8 as shown in the schematic diagram. For the first and second stage, it is used to provide better voltage gain and voltage swing respectively. Transistors M6 and M7 are used as a push-pull amplifier where M6 and M7 are NMOS and PMOS transistors respectively.

In this type of OTA, one major concern is regarding its stability [9]. There are various methods to resolve these issues. Here Miller compensation is used as per requirements. By selecting the proper aspect ratio of each transistor, the required specification can be achieved. Also, PMOS inputs are selected for low noise requirement in this topology.

## 4. DESIGN METHODOLOGY AND IMPLEMENTATION

In this section, the implementation and simulation of the biopotential amplifier, as well as differential amplifier and two-stage OTA, are represented. All the simulations are carried out in Cadence Virtuoso with 180nm technology. Also, the comparison with other implementation from different good literature is discussed.

In this work, the chopper-stabilization method is used with the bandpass response in feedback to achieve better performance. The configuration is shown in figure 8. It shows an operational transconductance amplifier (OTA) with a chopper at the input and out and bandpass filter at the feedback which is desired for such applications.

In designed architecture, to eliminate the extra filtering stage at the output of the demodulator, an OTA is used. By this way, the demodulator works on the output current of the operational transconductance amplifier is processed by the $C_{out}$.

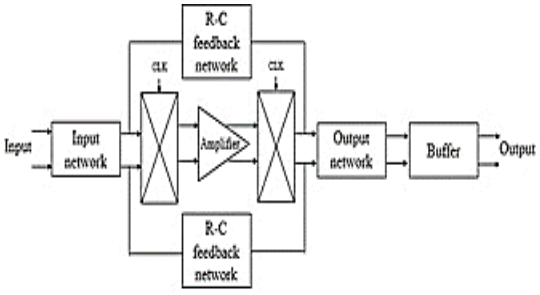


Figure 8. Block diagram of an implemented Biopotential Amplifier for ECG/EEG recording

In designed architecture, to eliminate the extra filtering stage at the output of the demodulator, an OTA is used. By this way, the demodulator works on the output current of the Operational transconductance. Due to the only one active block i.e. OTA, this design has the benefit of lower power, lower noise and simple to design. In the subsequent subsection, the mathematical model with the required analysis and simulation is presented. Also, the comparative analysis of designed architecture is shown for the biomedical applications.

### *A. Design consideration and Simulations*

The loop gain of design is given by multiplication of DC gain with feedback factor,

$$LG(S) = \frac{A_o\left(s+\frac{1}{R_2C_2}\right)\left(s+\frac{G_m}{A_mC_{out}}\right)}{C_1\left(s+\frac{1}{R_pC_1}\right)\left(s+\frac{G_m}{C_{out}}\right)} \quad (1)$$

$A_{ol}$ is open-loop gain of OTA which is given by,

$$A_o = G_mR_{out} \quad (2)$$

The closed-loop transfer function H(s) of the designed architecture is given by,

$$H(S) = \frac{A_ms}{\left(s+\frac{1}{R_2C_2}\right)\left(s+\frac{G_m}{A_mC_{out}}\right)} \quad (3)$$

Mid-band gain of the designed architecture is derived by the ratio of input capacitance and feedback capacitance

$$A_m = \frac{C_1}{C_2} \quad (4)$$

Also, the lower and higher cutoff frequency is given by

$$\omega_{LCF} = \frac{1}{R_2C_2} \quad (5)$$

$$\omega_{HCF} = \frac{G_m}{A_mC_{out}} \quad (6)$$

### *B. Simulation of the mathematical model*

The resultant transfer or closed-loop function of the designed architecture is given by

$$\frac{V_o}{V_{in}} = \frac{sC_1}{\left[\frac{s^2 C_{out}}{G_m}(C_1+C_2) - s\left(\frac{C_{out}}{G_m}\left(\frac{1}{R_p}+\frac{1}{R_2}\right)+C_2\right) - G_2\right]} \quad (7)$$

The Bode analysis is plotted for various values of the feedback resistance by considering a very high parasitic resistance.

The plot in figure 9 shows the response of frequency with the variation of the feedback resistance ($R_f$) for a different value of frequencies. From the plot, the idea about the values of feedback resistance and parasitic resistance are can be taken. So, for coupling and filtering, the better tuning of passive elements is there.

Also, these elements are important parameters as the chopper stabilization method is employed and also in feedback, bandpass response is required. But, the layout consideration of all the passive elements is important. So other alternatives to the design of passive elements are also very fruitful in such design. Due to chopper stabilization, the parameters like input impedance, offset and output ripple generate the trade-off. So, the value of Cin and $F_{chop}$ is properly selected to mitigate this issue.

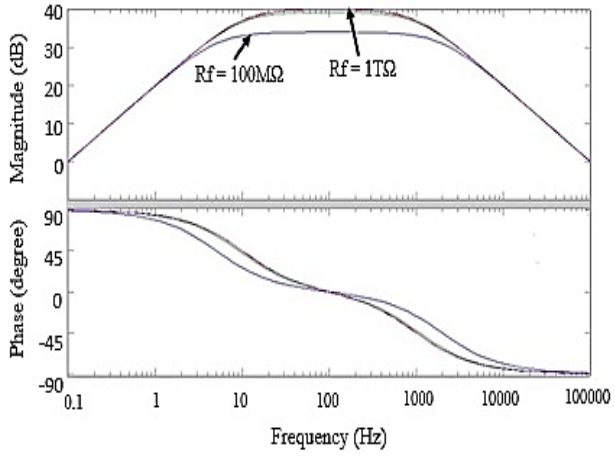


Figure 9. Frequency analysis with variation in feedback resistance

From this plot, to generate a better response, the high value of the feedback resistor is required. However, the size of the feedback resistor is increased and so, the size of the input capacitance is also increased to get high-frequency pole. The feedback resistance is taken as 1GΩ in this design as per figure 9.

### *C. Design consideration of chopping frequency*

The selection of chopping frequency is important to make sure the modulated signal is not attenuated by the frequency response of an amplifier; the chopping frequency is selected to be lesser than the 3-dB bandwidth of the amplifier [6].

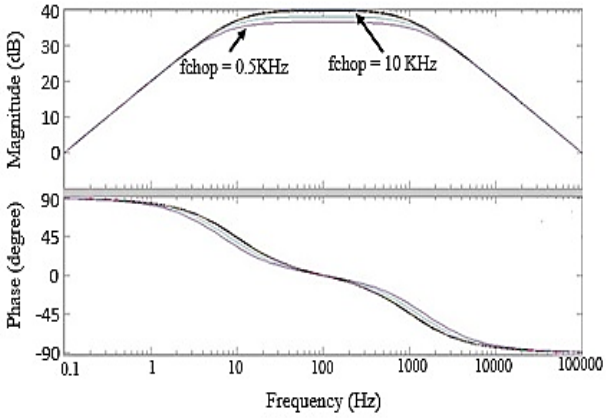


Figure 10. Frequency analysis with variation in chopping frequency

The smallest noise depends upon the selection upon the chopping frequency [9]. To ensure the modulation of flicker noise band and minimizing problems of noise folding and reduction in input impedance as it depends inversely on the chopping frequency, the selection of the chopping frequency is made very carefully. Chopper frequency is chosen in between the flicker noise corner and 3-dB corner of an amplifier. From figure 10, the chopping frequency in this design is taken as 1KHz.

### *D. Design consideration of Input modulator*

Input modulator is one of the critical and important design issues. Due to the switching operation, charge injection is there due to which the spikes are generated. These spikes are for the residual offset at the output as it is also amplified and demodulated. However, if the OTA is designed with a proper bandwidth, then this effect can be reduced.

### *E. Design consideration of Input capacitance*

The input capacitance of the amplifier is mainly responsible for the parasitic. The optimization in the layout to minimize the input impedance requires more effort.

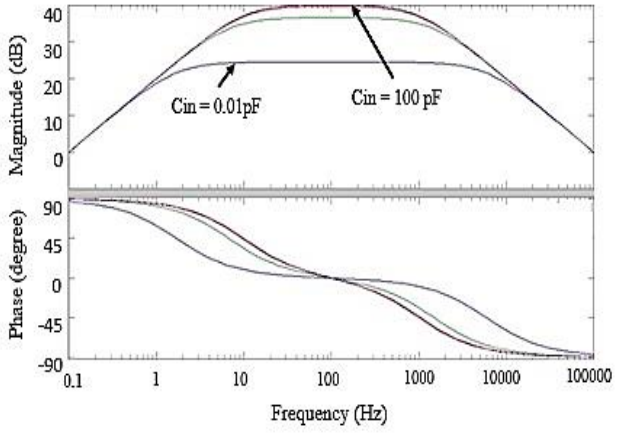


Figure 11. Frequency analysis with variation in input capacitance

The size of the transistors is an important factor for the input capacitance. For the large area, the larger the input capacitance. In low noise amplifier designs, the input transistors are considered as large as possible to achieve very small noise[10]. Also, to design 40 dB OTA and high pass pole, the higher $C_{in}$ is required. This comes at the cost of the parasitic capacitance.

In figure 11, the frequency response with the variation in input capacitance is shown. From this, the idea about the value of input capacitance can be taken. From this result, the value of input capacitance is considered as 10pF.

The consideration of Fchop and Cin is very crucial in this design as input impedance must be high but Fchop and Cin are inversely proportional to Zin.

## 5. TRANSISTOR LEVEL IMPLEMENTATION AND ANALYSIS

In this section, the circuit level implementation of a biopotential amplifier is discussed. The schematic diagram of the biopotential amplifier is mention in figure-12. The values of parasitic components and chopping frequencies are taken as per Matlab simulation which was discussed in the previous section.

All the individual blocks – clock generator circuits, chopper modulator and chopper demodulator, OTA with CMFB are shown in circuit schematics. A two-stage op-amp is used as a buffer. In buffer design, PMOS is used at the input device to improve the noise performance Also, Miller compensation is used to resolve the stability issue. Later, symbolic representation of all the blocks which is used to implement is shown. Further, the simulation results of the proposed designed are also shown. The simulations are carried out in Cadence using 180nm technology as it is more suitable for analog design as per the current state of the art. As in lower technology nodes, it is more difficult to handle non-linearity in analog design compare to digital design. So,180nm is used in this design compare to lower technology nodes.

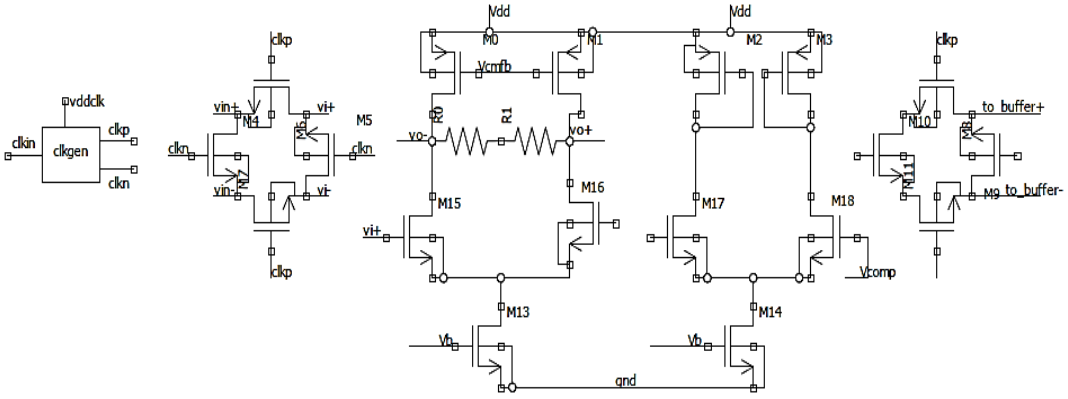


Figure 12. Schematic diagram of Chopper stabilized Biopotential amplifier

In figure 12, the overall schematic diagram of the above circuit is shown for the analysis purpose. All the necessary analysis is shown in the upcoming Figs. In design right now, thee passive elements like capacitor and resistance are used with the higher values which required more amount of area in layout design.

As of alternatives to this, T-network resistor [3] can be used to get the higher value of the resistance with the optimized layout. But as these active elements are using biasing circuits, which is to be designed properly.

Here, AC, DC, transient and noise analysis are carried out and all the observed and calculated results are mentions also. Also, the simulation of all individual blocks is done. The theoretical specifications and obtained specifications are also shown in tabular form. Those specifications are selected for the ECG and EEG acquisition requirements/

In figure 13, the schematic diagram of the chopper is shown and also in Fig 15, the simulated result for the modulation is shown.

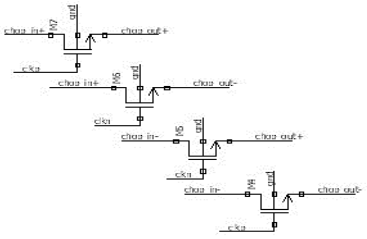

Figure 13. Circuit schematic of the chopper

For the modulator, while designing the transistors, smaller the length is required to deal with parasitic and ON resistance of switches. The on resistance of a switch also becomes a noise source and it must be low enough.

So, the designing of the switch is also a very important issue. The transmission gate or CPL switch is referred to either a pMOS or an nMOS switch to reduce the spikes due to charge injection. However, the parasitic capacitance is included which further reduces in input impedance. Thus, a choice of a simple NMOS is chosen which provides a good balance between these limitations in this design [10].

The transient analysis to verify the design is shown in figure 14 which represents the output modulated waveform which is given to the OTA for the amplification purpose.

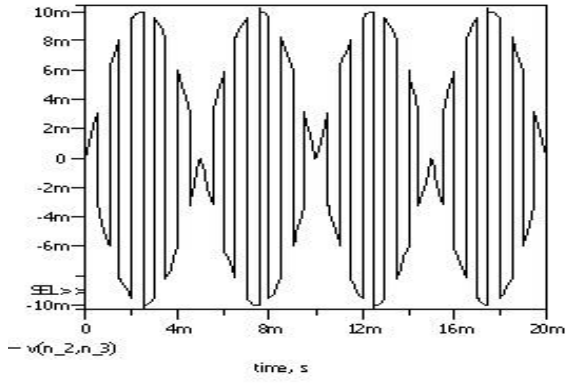


Figure 14. output of the chopper circuit

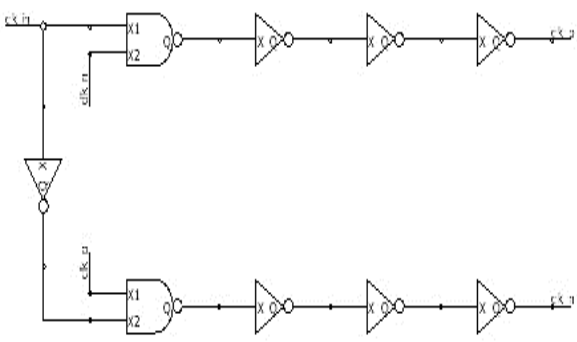


Figure 15. Circuit schematic of the clock generator circuit

To design the clock generator circuit, the combinations of the NAND and inverter gate, is required. Also, these gates are designed to produce minimum delay. This circuit will produce non-overlapping circuit with 50% of the duty cycle. The result is shown in figure 16.

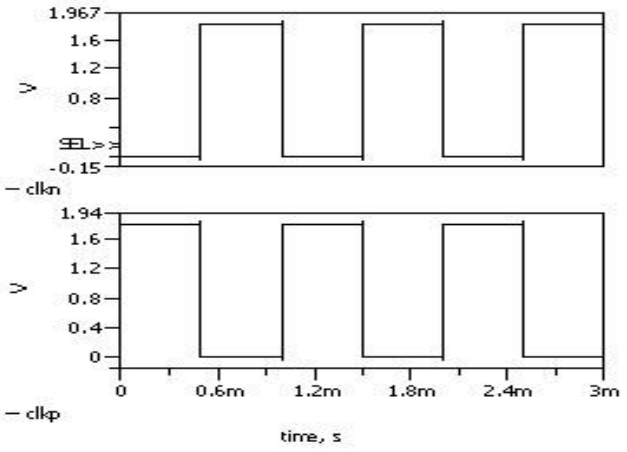


Figure 16. Generation of non-overlapping clock

In figure 17, the single-stage differential amplifier as an OTA is shown with the CMFB circuit for a specification mention in table 2

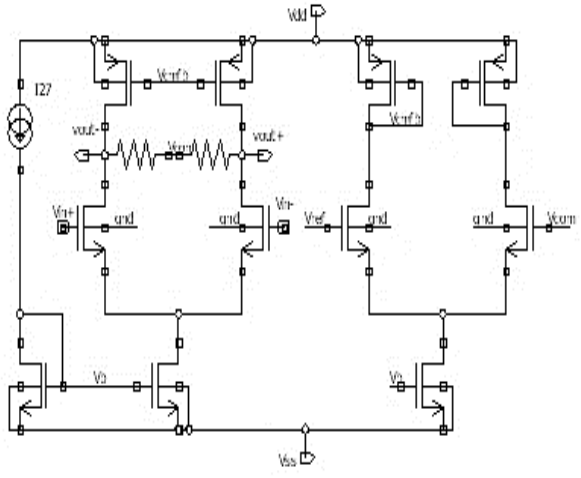


Figure 17. Circuit schematic of OTA with CMFB

TABLE 2. SPECIFICATION OF OTA

| Specifications | Given specification | Obtained Specification |
|---|---|---|
| Power supply | 1.8V | 1.8V |
| DC gain | >40dB | 37.3dB |
| CMRR | >80dB | 81.6dB |
| Power Dissipation | <10µW | 1.8µW |
| ICMR | -1.2V-1.2V | -1V-1.2V |
| CL | 10pF | 10pF |
| Slew Rate | >2v/µS | 2v/µS |
| Input referred noise | <20nV/$\sqrt{Hz}$ | 12nV/$\sqrt{Hz}$ |

In figure 18, the two-stage differential amplifier for the buffer is shown for a specification mention in the table3. Here, the specifications are taken into account for the application of recording the ECG or EEG signals. For that, the parameters like noise, power, CMRR and offset are very crucial. From all these parameters, in this work, the main focus is noise and power balance as there will be always a trade-off. Here, the 180nm technology with the power supply of 1.8V is used.

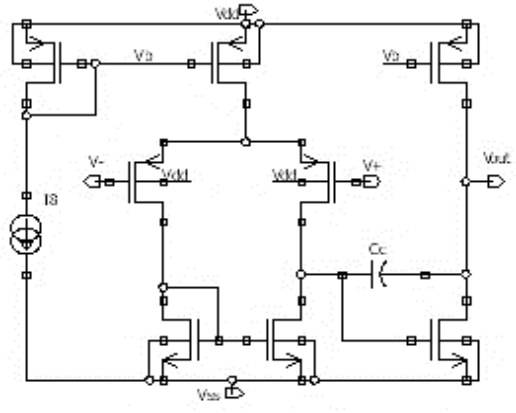


Figure 18. Circuit schematic of two-stage op-amp

In table 3, the specifications of the two-stage op-amp are shown.

TABLE 3. SPECIFICATION OF TWO-STAGE OP-AMP

| Specifications | Given specification | Obtained Specification |
|---|---|---|
| Power supply | 1.8V | 1.8V |
| DC gain | >70dB | 75dB |
| CMRR | >80dB | 83.9dB |
| Power Dissipation | <20µW | 6µW |
| Input referred noise | <20nV/$\sqrt{Hz}$ | 19nV/$\sqrt{Hz}$ |
| ICMR | -1.2V-1.2V | -1.2V-1.2V |
| CL | 10pF | 10pF |
| Slew Rate | >2V/µS | 2V/µS |

In figure 19 to figure 22 the simulated results of the biopotential amplifier are shown which represented the DC, AC, transient and noise analysis.

All such kind of analysis needs a different setup for the input source and based on that the simulation is done. All the analysis of design is important to observe the behaviour of the system and to design the front end of the system for biomedical application.

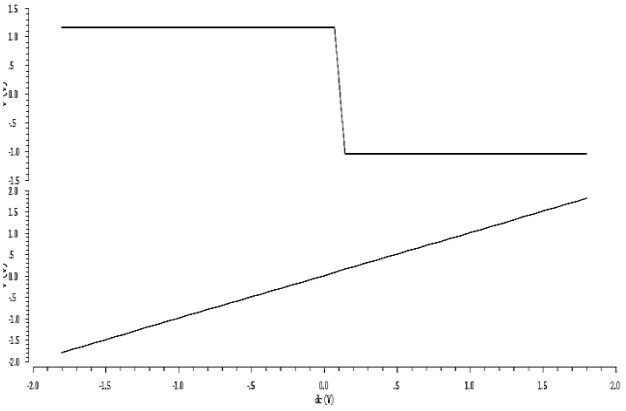

Figure 19. DC analysis

In figure 20, the AC analysis of IA is shown, which represents the gain of 40dB. Also, here two-stage op-amp with PMOS input is designed to reduce the noise and Miller compensation method is applied for stability. After applying the compensation method the phase margin is 61°. Instead of the two-stage op-amp, the folded cascode op-amp also can be used at the cost of some output swing. So as per the specifications, proper topology can be utilized.

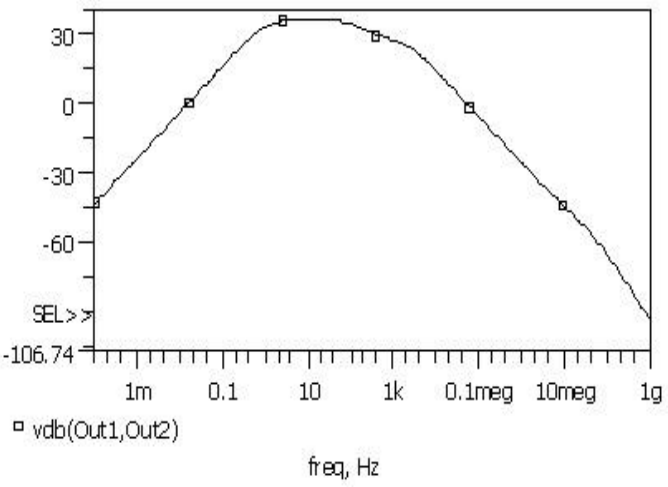


Figure 20. AC analysis

In figure 21, noise analysis is shown with input-referred noise of 31nV/$\sqrt{Hz}$ at 100Hz frequency with THD is less than 15% up to the third harmonic with good SNR.

The low noise amplifier is one of the important criteria for such kind of applications. The noise can be reduced by making input transistor large but due to that the parasitic of the device is increased, so chopper stabilization technique is introduced here.

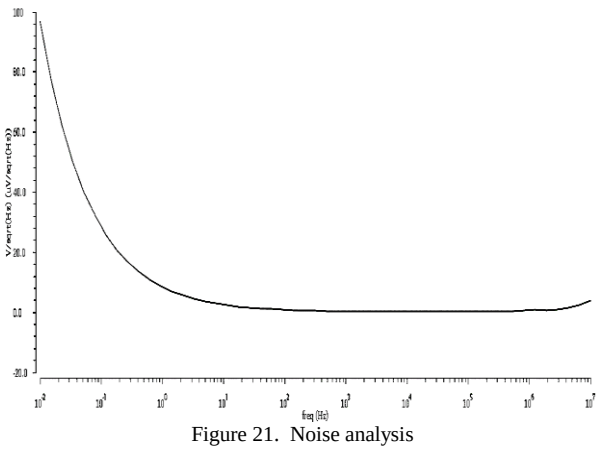

Figure 21. Noise analysis

In figure 22, the transient analysis of the given biopotential amplifier is shown in which input signal is given as 1mV of range with 100Hz frequency and output is represented as 100mV with the gain of 40dB which is desired for the recording of the ECG signal.

Also, in this design, the bandwidth of the amplifier is slightly higher than the chopper frequency but due to chopper stabilization, the input impedance is going to be reduced. So various technique can be used to improve the results.

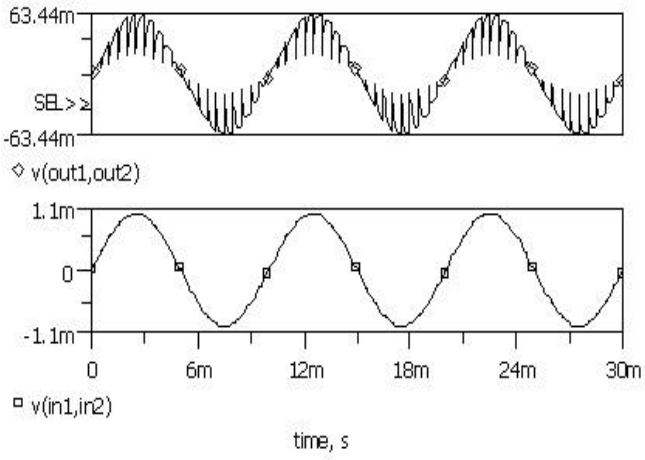


Figure 22. Transient analysis

### A. *Comparative Analysis*

Here, in table 4, the comparative analysis of designed biopotential amplifier is shown with different kinds of literature and also the outcome of this design is presented. Still, the power consumptions can be modified by using active resistance instead of passive resistance and other architecture optimization.

For the comparison, mostly the literature from the solid-state circuits is taken. Also, the latest literature regarding biomedical applications are taken into account but not all are mention over here.

TABLE 4. COMPARATIVE ANALYSIS OF DIFFERENT BIOPOTENTIAL AMPLIFIER

| Parameters | [8] | [11] | [12] | [13] | [14] | [15] | [16] | **This work** |
|---|---|---|---|---|---|---|---|---|
| Process | 180nm | 180nm | 180nm | 180nm | 180nm | 180nm | 180nm | 180nm |
| Supply | 1.8V | 1.8V | 1.25V | 1V | 1.8V | 1.8V | 2.7V | 1.8V |
| Gain | 34.7dB | 40dB | - | 60dB | 41dB | 30dB | 40dB | 40dB |
| Power | 4.2µW | - | 2.125µw | 3.5µW | 2µW | 75µW | - | 8µW |
| Bandwidth | 100Hz | 3.5KHz | 10KHz | 100Hz | 200Hz | 1KHz | 2KHz | 1KHz |
| CMRR | 71.5dB | 100dB | 85dB | 60dB | 100dB | 100dB | 51dB | 84dB |
| Noise ($nV/\sqrt{Hz}$) | 250 | 39 | 45 | 130 | 95 | 75 | 3.76 | 31 |

### B. *A layout of the overall design*

In figure 23, the basic floor plan of design is shown.

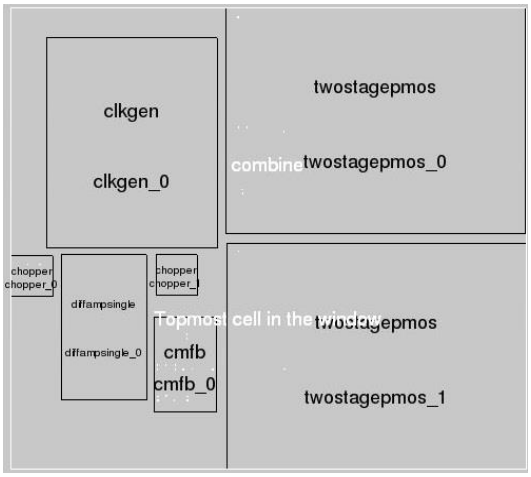


Figure 23. Floor plan of the design

In figure 24 the layout design is shown. The layout is designed in Magic tool with 180nm technology with proper matching methods of the device with taking care of minimum parasitic.

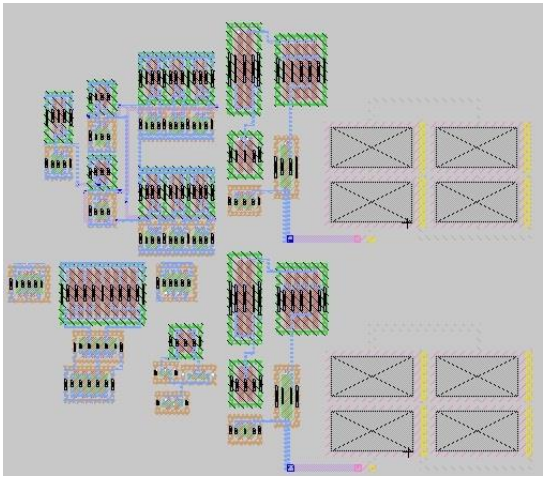

Figure 24. Layout of design

## 6. CONCLUSIONS

The designed biopotential amplifier is a chopper-based biopotential amplifier to achieve the desired balance between the specifications especially noise and power. This architecture is optimized to achieve the DC gain of 40 dB, CMRR of 84 dB and the power dissipation of 8 µW with total input noise of 31nV/$\sqrt{Hz}$ . The designed architecture is also optimized to give optimum noise performance using PMOS input stages. Also due to only one OTA in front-end readout part, the overall power consumption is less. Further, the active resistors can be used to optimize the design to save the area and noise parameter. The above-mentioned parameters are measured by carrying out simulations in Cadence virtuoso EDA tool with 180nm technology.

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