International Journal of Computing and Digital Systems
ISSN (2210-142X)
Int. J. Com. Dig. Sys. 12, No.1 (Sep-2022)

https://dx.doi.org/10.12785/ijcds/120162

True Single Phase Clock based UP-DOWN Counter using GDI Cell for Low Power Applications

Jitesh Singh Chauhan*[1] and Ram Chandra Singh Chauhan[2]

[1] M. Tech Scholar, Microelectronics, Institute of Engineering and Technology, Lucknow, India.
[2]Associate Professor, Department of Electronics and Communication Engineering, Institute of Engineering and Technology, Lucknow, India

Received 01 Nov. 2020, Revised 03 May. 2022, Accepted 19 Jun. 2022, Published 30 Sep. 2022

Abstract: The designing of low power circuits has been a constant area of research in integrated circuits. As the technology advances, the electronic systems are becoming battery operated hence the efficient utilization of power is necessary because of limited power sources. In computers, the memory requirement is unavoidable, so flip-flops are used as digital data storage unit. Flip-Flops are sequential circuits whose response is controlled by the clock signal. While studying the internal circuitry of the flip-flops we can observe that the power dissipation depends mostly on the switching activity of the circuit due to clock signal. Here we have proposed a reset-abled flip-flop which is fast in performance, has low power dissipation at high data activity and requires less area on silicon chip. Flip-Flop finds numerous applications like counters, shift registers, memory elements etc. Here we have proposed an UP-DOWN counter using gate diffusion input (GDI) cell, its performance is evaluated and compared with conventional method-based counters. The circuits are simulated in standard 90 nm CMOS process technology in Cadence Virtuoso EDA tool. The performance analysis of the proposed flip-flop at 400 MHz clock frequency shows that the power dissipation is 187.1 nW, signal propagation delay is 127.15 ps and area requirement is 81.8 μm^2. Also, at 1 GHz clock frequency, the proposed counter dissipates 1040.55 nW power and it requires 388.2 μm^2 area on IC chip.

Keywords: Low Power, VLSI, UP-DOWN Counter, TSPC, GDI cell, CMOS Circuits

1. Introduction

Counters are used to record the number of occurrences of an event. They also find application in circuits like frequency dividers, analog-to-digital converters (ADCs), timers etc [1]–[4]. As the devices are becoming portable and battery operated in nature, the demand of low power consuming systems is increasing rapidly [5], [6]. In CMOS circuits, the transistors are used as switches that are ON or OFF depending on the voltage applied at their gate input terminal. The power in CMOS circuits are categorized as static power and dynamic power [7]. Static power dissipation occurs when there is no input applied to the circuit i.e., the circuit is in idle condition. The sources of static power are p-n junction reverse bias current, subthreshold leakage current, tunneling through gate oxide, hot carrier injection etc [8]. On the other hand, the dynamic power dissipation is due to the flow of current when the transistors switch from one state to another (ON to OFF and vice-versa) and it is classified into short circuit power dissipation and switching power dissipation. In digital circuits, during logic transition, there exists a path between VDD and ground when PMOS and NMOS transistors are ON simultaneously, causing short circuit current conduction that leads to short circuit power dissipation [9]. Also, switching power dissipation represents the power dissipation in the course of a switching event. This means that the output node voltage of a CMOS logic gate makes an energy consuming transition [10]. In digital CMOS circuits, dynamic energy is dissipated when power is drawn from the power supply to charge up the output node capacitance. During the charge-up phase, the output node voltage normally makes a complete transition from 0 to VDD and the power dissipated in this transition is called switching power dissipation. It is the dominant power dissipation in sequential circuits because many internal transistors are driven by the clock signal which continuously toggles from one state to another causing huge switching power dissipation in the circuits [11], [12]. In this paper we have proposed a reset-abled flip-flip which is power as well as area efficient. The

E-mail address: cjitesh6@gmail.com, rcschauhan@ietlucknow.ac.in

proposed flip-flop is used to design a 3-bit counter which can perform both UP counting and DOWN counting with the help of a GDI cell. The designs are simulated and compared with the conventional circuits. The proposed designs are faster in performance, high reduction in power dissipation is achieved and they utilize lesser transistors.

The paper is organized as follow: section 2 gives an overview of GDI cell, in section 3 the conventional flip-flop is discussed, the proposed flip-flop is mentioned in section 4, the proposed counter is described in section 5, simulation work of the proposed and existing circuits is shown in section 6, the results and the comparison of circuit performance parameters are given in section 7 and then the conclusions and future scope of this work are mentioned in section 8 of the paper.

2. Overview Of GDI Cell

A gate diffusion input cell looks similar to a CMOS inverter. In CMOS circuits the p-block (network consisting of PMOS transistors) and the n-block (network consisting of NMOS transistors) are used to pull-up and pull-down a node voltage to VDD and ground respectively. In case of an inverter the gate terminals of both PMOS and NMOS transistors are connected together and the source terminals of PMOS and NMOS transistors are connected to VDD and ground respectively. The GDI cell is diagrammatically similar to CMOS inverter but the voltages VDD and ground are replaced by the input signals A and B as shown in Fig. 1. The GDI cell can be used to implement the output function of the logic gates, multiplexer, half adder etc. and its combination can implement bigger circuits like full adder, full subtractor, comparators etc [13].

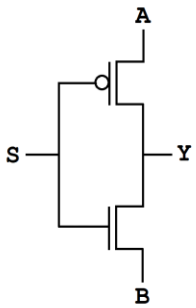

Figure 1. GDI Cell Circuit Diagram

This technique uses less number of transistors and power requirement is low as compared to CMOS based circuits [14]. From Fig. 1, we can observe that the GDI cell has three inputs A, B, S and the output Y. For our design we are using the GDI cell as a 2:1 multiplexer (MUX) and the reason for this will be discussed in the following sections. A multiplexer is a data line selection device, also called as many to one device because it connects the output terminal to different input terminals depending upon the select control signal [15]. For a 2:1 multiplexer the inputs to the MUX are two, one control (select) signal and one output. A conventional transmission gate based 2:1 MUX is shown in Fig. 2 and its standard symbolic representation is given in Fig. 3. The inputs A and B are passed onto the output Y on the basis of logic level of S (select) signal.

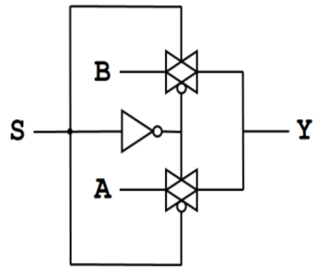

Figure 2. Transmission Gate based 2:1 MUX

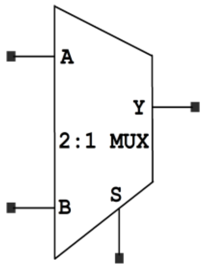

Figure 3. Symbolic Representation of 2:1 MUX

The functioning of multiplexer can be understood by the Table I where all the input combinations are illustrated. Later on, we shall compare its functionality with the GDI cell based MUX.

TABLE I. Truth Table of 2:1 MUX

Select Input	Data Input		Output
S	**A**	**B**	**Y**
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Y=A when S=0

Y=B when S=1

The Table I shows that when S = 0, the input A is passed onto the output Y and when S = 1, the input B is passed onto the output Y. The similar function is implemented by using a GDI cell and its working is illustrated in Table II. The inputs A and B are applied to the source terminals of PMOS and NMOS transistors respectively and the select signal S is applied to the common gate terminal of the cell as shown in Fig. 1. When S = 0, the PMOS is ON, Y is connected to the signal A and when S = 1, the NMOS is ON, Y is connected to the signal B.

TABLE II. FUNCTIONAL TRUTH-TABLE OF GDI CELL AS 2:1 MUX

Select Input	Transistor		Output
S	NMOS	PMOS	Y
0	OFF	ON	A
1	ON	OFF	B

The number of transistors utilized in designing the MUX as shown in Fig. 2 are six but the similar function is implemented by using gate diffusion input technique that requires only two transistors. This reduces the area requirement on silicon chip as well as the power dissipation by the circuit.

3. CONVENTIONAL FLIP-FLOP

Flip-Flops are data storage elements in digital circuits that contain information in the form of bits [16], [17]. The response of the flip-flop is either LOW (logic 0) or HIGH (logic 1) hence it is a bistable circuit. The output depends upon the present input and previous response of the circuit. The data latching is controlled by the clock signal which makes the flip-flop a sequential circuit [18]. The most commonly used flip-flop is D flip-flop (DFF) where D signifies Data or Delay. It is highly used in memory devices, counters and shift registers. The typical block diagram of a D flip-flop is shown in Fig. 4 where we can observe that the input pins D and CLK are for data and clock signals respectively and the output pins Q and Qb (or Q') are complements of each other.

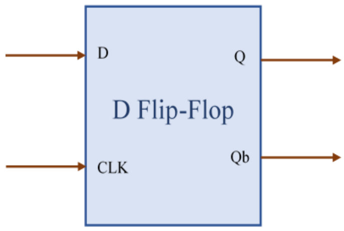

FIGURE 4. BLOCK DIAGRAMMATIC REPRESENTATION OF D FLIP-FLOP

Here we shall look at the conventional transmission gate based D flip-flop (TGDFF), its circuit diagram and working. It has a master-slave configuration and the data latching in master or slave latch is commanded by the two phases of the clock signal [19]. The circuit diagram of TGDFF is shown in Fig. 5, where we can see that the flip-flop is designed by using transmission gates and CMOS inverters. It works on dual phase clock mechanism i.e.; the master clock CL is connected to two inverters I7 and I8 to generate CLK and CLK' signals that are out of phase by 180°. These two clock signals are used to activate the master and slave latches.

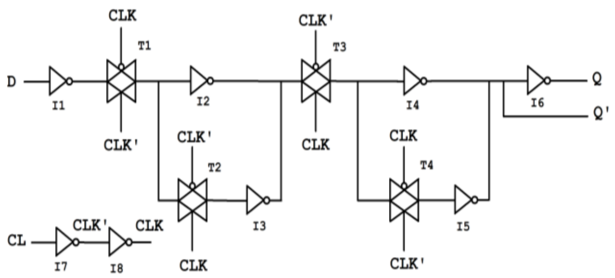

FIGURE 5. CONVENTIONAL D FLIP-FLOP

The transmission gates T1, T2 and inverters I2, I3 resemble the master configuration and similarly the transmission gates T3, T4 and inverters I4, I5 resemble the slave configuration. When CLK = LOW (logic 0), CLK' = HIGH (logic 1), T1 is ON and the data is passed onto the master latch meanwhile T3 is OFF, hence the slave latch is inactive. Now when CLK = HIGH (logic 1), CLK' = LOW (logic 0), T3 becomes ON and the data present in the master latch is passed onto the slave latch and the final output is received at Q and Q' terminals of the flip-flop.

The TGDFF uses total 24 transistors out of which 12 transistors are directly driven by the clock signal. Due to more number of transistors connected with the clock, the internal circuitry of the flip-flop experiences continuous toggling that causes huge switching power dissipation. This phenomenon is redundant when the data activity is zero i.e., no data is applied at the input of the flip-flop but the circuit keeps dissipating power due to the applied clock signal [20]. Also, the number of transistors required to implement this circuit are more in number hence large area would be required on silicon chip.

4. PROPOSED D FLIP-FLOP

A lot of research is being done to design a high-performance D flip-flop because it is an essential part in every electronic system [21]–[23]. Here we have proposed a rising (positive) edge triggered dynamic CMOS circuit-based D flip-flop whose response depends upon the transient behavior of the node capacitances of the circuit. The output of the conventional circuits relay on the steady state behavior of the logic gates which leads to the sluggish response of the circuit. It is obvious that the transient response of a system takes less time as compared to the steady state response hence the proposed design performs faster in comparison with the existing designs. Fig. 6 shows the circuit schematic of the proposed flip-flop.

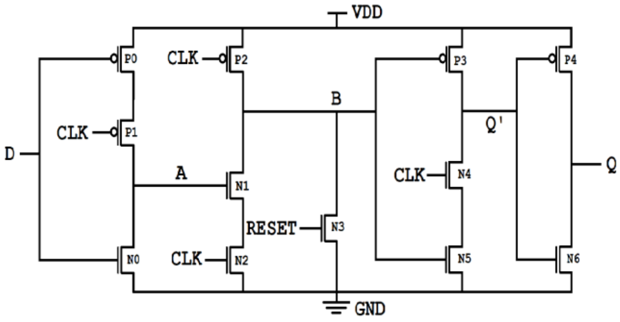

FIGURE 6. PROPOSED D FLIP-FLOP

The flip-flop is dedicated specially for counter applications hence we have designed a reset-abled D flip-flop. Apart from inputs D and CLK, a RESET input is given in the circuit which is connected to the pull-down NMOS transistor (N3) that is used to clear the flip-flop. When RESET = HIGH (logic 1), N3 is ON and it pulls down the node B voltage to ground (LOW). Now when B = LOW (logic 0), the PMOS transistor P3 is ON and Q' becomes HIGH and this logic level gets inverted by the inverter constituting P4 and N6 transistors and finally Q becomes LOW (logic 0). This function is necessary for forcing the flip-flop to a certain logic level so as to eliminate the abnormal response of the counter designed by using this flip-flop. The functional truth table of the proposed flip-flop is given in Table III where the input-output combinations along with the state of the transistors are mentioned.

Now we shall look at the concept of power in CMOS circuits, its classification and the parameters that affect it. The power dissipation is divided into two types:

- Static Power Dissipation
- Dynamic Power Dissipation

We have already discussed that the static power is dissipated when the circuit is in idle condition and it is due to the leakage current. The static power dissipation can be mathematically represented as:

$$P_{static} = \sum_i I_{OFF_i} * V_{DD} = I_{OFF_T} * V_{DD} \quad (1)$$

where

I_{OFF_i} = leakage current component when input is zero.

I_{OFF_T} = total leakage current.

The leakage currents are due to the flaws in transistor fabrication process and they are of very low magnitude. The dynamic power dissipates due to the charging and discharging of load capacitance as well as node capacitance. The formula for the calculation of dynamic power dissipation is:

$$P_{dynamic} = \alpha_L C_L {V_{DD}}^2 f_{clk} + \sum_k \alpha_k C_k V_{DD}(V_{DD} - V_t) f_{clk} \quad (2)$$

where:

C_L = load capacitance

α_L = switching activity at the load.

C_k = kth node capacitance

α_k = switching activity at kth node

V_t = threshold voltage of the transistor

f_{clk} = operating clock frequency

It should be noted that the power dissipation (static and dynamic) depends upon the supply voltage VDD so as VDD increases, it would lead to more power dissipation in the circuit. From (2), we can observe that the clock frequency also affects the power dissipation. As we increase the clock frequency, the power dissipation would be more. These parameters are taken into consideration at simulation level and the optimum values are chosen to design low power circuits.

5. PROPOSED UP-DOWN COUNTER USING GDI CELL

Here the proposed flip-flop is utilized to design a low power asynchronous counter. An n-bit counter consists of n number of flip-flops and it counts from 0 to 2^n-1. The counters are classified into two types: synchronous counters and asynchronous counters. In synchronous counter, the clock signal is applied to all the flip-flops simultaneously while in case of an asynchronous counter,

TABLE III. FUNCTIONAL TRUTH-TABLE OF PROPOSED FLIP-FLOP

Input			Transistors												Output	
RESET	D	CLK	P0	P1	P2	P3	P4	N0	N1	N2	N3	N4	N5	N6	Q'	Q
1	X	X	X	X	X	ON	OFF	X	X	X	ON	X	OFF	ON	1	0
0	0	0	ON	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	1	0
0	0	1	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	ON	1	0
0	1	0	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	1	0
0	1	1	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF	0	1

the clock signal is applied to the first flip-flop only and the output of the first flip-flop is considered as least significant bit (LSB). Here the output of previous flip-flop acts as clock signal for the next flip-flop. The asynchronous counters consume less power due to the fact that in this approach, the transistors triggered by the clock signal are less in number. In synchronous counters, all the flip-flops are clock triggered and therefore more number of transistors experience switching due to clock signals. The counters are also expressed in terms of the way counting is done for e.g., in UP counters, the output sequence is from 0 to 2^n-1 and in DOWN counters, the output sequence is from 2^n-1 to 0. The representation of a 3-bit UP counter is given in Fig. 7. To design a counter, we need a flip-flop that toggle its state on every rising or falling edge of the clock signal. Here the D flip-flop is used in toggle mode by connecting the complemented output Q' (or Qb) to the input D of the flip-flop. For e.g., assume the flip-flop is clear i.e., Q = 0 that means Q' = 1 and therefore D = Q' = 1. On the next clock triggering Q = 1, Q' = 0 and D = Q' = 0. This cycle continues and a D flip-flop can be used in toggle mode configuration.

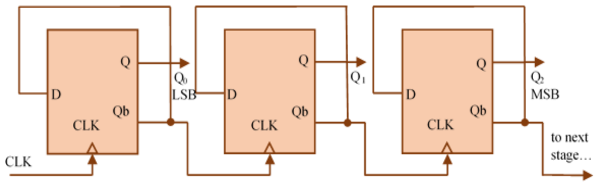

FIGURE 7. AN ASYNCHRONOUS UP COUNTER

From Fig. 7, we can see that the clock signal CLK is applied to the first flip-flop and the output Qb of the flip-flop acts as a clock signal for the next flip-flop.

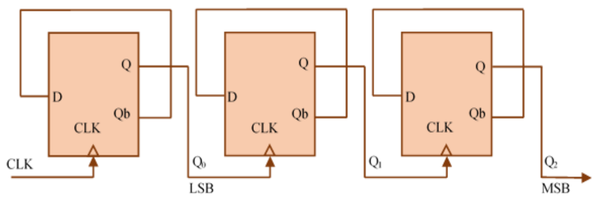

FIGURE 8. AN ASYNCHRONOUS DOWN COUNTER

Fig. 8 represents a 3-bit DOWN counter where we can observe that the output Q of the flip-flop acts as clock signal. Now we shall design a circuit that can perform both UP counting and DOWN counting by using the proposed flip-flop. The idea is to club the output signals Q and Qb of the flip-flop and apply them to a data line selector device. The inputs to the data line selector will be Q and Qb and its output will be connected to the clock input of the next flip-flop. A control signal is used to decide which output Q or Qb is to be selected and passed onto the output port of the data line selector device from where it can be connected to the clock input of the flip-flop.

In our proposed counter we are using the GDI cell in MUX configuration to achieve the data line selection property. In Fig. 9, the proposed 3-bit counter is given where we can see that both the outputs of the flip-flops are applied to data line selector device and its output is connected to the CLK terminal of next flip-flops. The output sequence of the 3-bit UP-DOWN counter is given in Table IV below.

TABLE IV. OUTPUT SEQUENCE OF 3-BIT UP-DOWN COUNTER

CLOCK (CLK)	OUTPUT					
	UP Counter			DOWN Counter		
	Q_2 (MSB)	Q_1	Q_0 (LSB)	Q_2 (MSB)	Q_1	Q_0 (LSB)
1	0	0	0	1	1	1
2	0	0	1	1	1	0
3	0	1	0	1	0	1
4	0	1	1	1	0	0
5	1	0	0	0	1	1
6	1	0	1	0	1	0
7	1	1	0	0	0	1
8	1	1	1	0	0	0

Now in order to verify the performance of the proposed designs, we have simulated them in 90 nm standard CMOS process technology using Cadence Virtuoso software and the parametric analysis of the circuits are also done. We have compared the proposed circuits with conventional circuits in terms of power dissipation, signal propagation delay, layout area and device utilization.

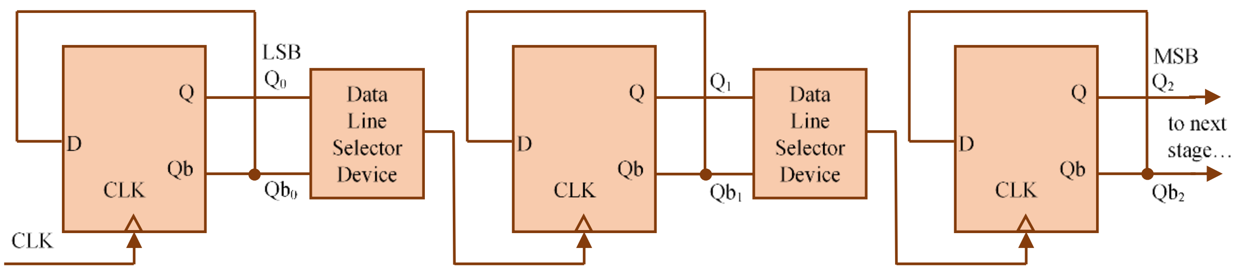

FIGURE 9. BLOCK DIAGRAM OF PROPOSED 3-BIT UP-DOWN COUNTER

6. SIMULATION WORK

Here we shall first look at the simulation of the proposed D flip-flop. Our aim is to design a high frequency flip-flop hence 400 MHz clock frequency is chosen. Standard generic process 90 nm library is used and the parametric analysis is recorded at room temperature.

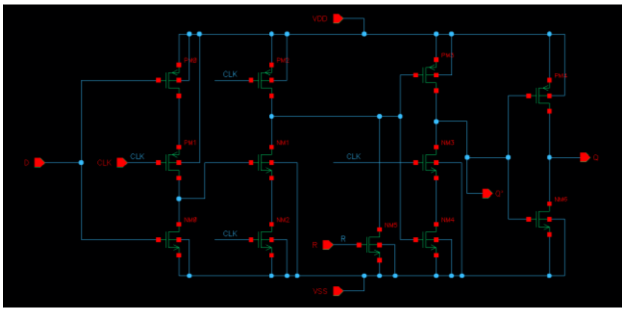

FIGURE 10. SIMULATED CIRCUIT SCHEMATIC OF PROPOSED D FLIP-FLOP

Proposed flip-flop as shown in Fig. 6 is simulated in Cadence Virtuoso EDA and its schematic is shown in Fig. 10. Now the transient analysis of the flip-flop is done which shows the waveforms of input signals D, CLK, output Q and power. The transient response is shown in Fig. 11 below.

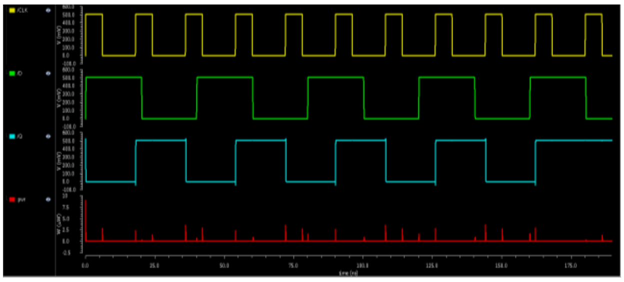

FIGURE 11. TRANSIENT RESPONSE OF THE PROPOSED D FLIP-FLOP

The proposed flip-flop is rising or positive edge triggered i.e., the data present at input D gets reflected at output Q upon the arrival of rising edge of the clock signal. In Fig. 11 the first waveform shows the clock signal CLK, then input D, the output Q is shown by third waveform and finally the transient power. The duty cycle of the clock is taken 33% to get a clear picture of data latching as shown in Fig. 11. The change in logic levels of Q can be observed on every rising edge of the clock signal and the output follows the input which verifies the operation of D flip-flop.

Now the proposed counter is simulated as shown in Fig. 12. The transient analysis of the counter is done which shows the output sequence of both 3-bit UP counter and DOWN counter as given in Fig. 13. In order to design a high frequency counter, we have taken 1 GHz clock frequency. It should be noted that at such a high frequency most of the existing flip-flops and counters fail to operate and show glitches in the response.

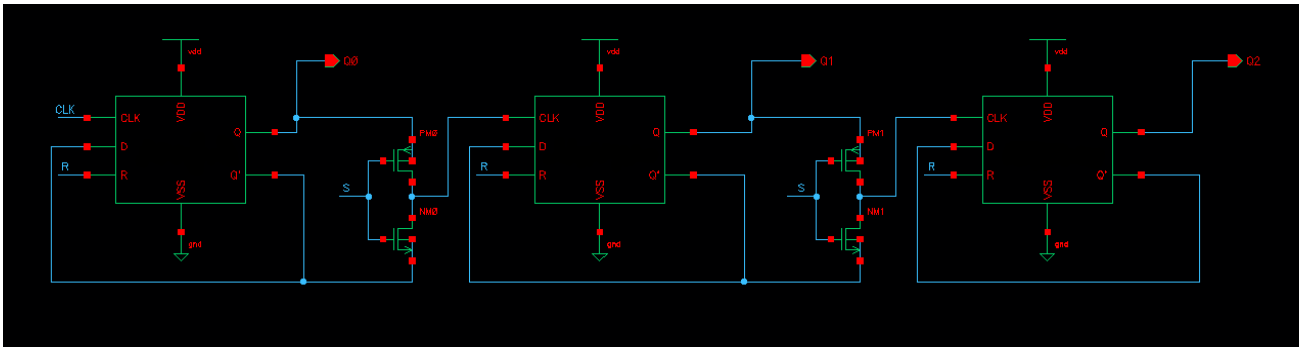

FIGURE 12. SIMULATED CIRCUIT SCHEMATIC OF PROPOSED UP-DOWN COUNTER

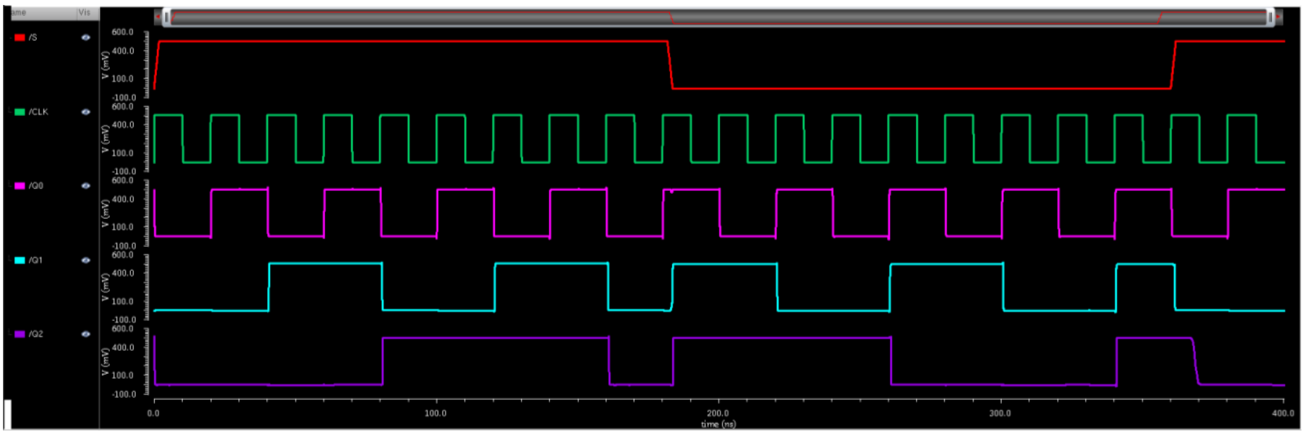

FIGURE 13. TRANSIENT RESPONSE OF PROPOSED UP-DOWN COUNTER

The flip-flop shown in Fig. 10 is converted into a square symbol and then it is used in designing counters as shown in Fig. 12 i.e., the square blocks we are seeing in Fig. 12 contains proposed D flip-flop which was given in Fig. 10. The flip-flops used in implementing counter are in toggle mode i.e., the output Qb (or Q') is fed to the input D of the flip-flop. Both the outputs Q and Qb (or Q') of the flip-flop are connected with the GDI cell. The control signal for the GDI cell is S which is connected to the gate input of the transistors and the output of the GDI cell is connected to the CLK input of the next flip-flop. Now when S = HIGH (logic 1), the NMOS transistor in GDI cell gets ON that causes Qb (or Q') to connect to CLK through NMOS transistor and hence the circuit performs UP counting ($Q_2Q_1Q_0$ = 000 to $Q_2Q_1Q_0$ = 111). Similarly, when S = LOW (logic 0), the PMOS transistor in GDI cell gets ON, Q gets connected to CLK through PMOS and the circuit performs DOWN counting ($Q_2Q_1Q_0$ = 111 to $Q_2Q_1Q_0$ = 000). The working discussed here can also be verified from the transient response of the counter as shown in Fig. 13 where waveforms of S, CLK, Q0, Q1 and Q2 are given from top to bottom.

7. Results and Discussion

After looking at the simulation of circuit schematics and transient responses of the proposed work, we shall now estimate the performance of the circuits in terms of power dissipation, delay, rise time, fall time and layout area. For comparison purpose, we have simulated the conventional D flip-flop (TGDFF) and then a 3-bit UP-DOWN counter consisting conventional flip-flop and 2:1 MUX as data line selector. These circuits are compared with the proposed designs in terms of different performance parameters. First, we shall see the timing estimation where parameters related to time i.e., delay, rise time and fall time are discussed. Table V shows the comparison of timing parameters.

TABLE V. COMPARISON OF TIMING PARAMETERS

S. No.	Design	Delay $t_{clk\text{-}Q}$ LOW to HIGH (ps)	Delay $t_{clk\text{-}Q}$ HIGH to LOW (ps)	Rise Time t_r (ps)	Fall Time t_f (ps)
1.	TGDFF	285	144.8	64.85	50.01
2.	**Proposed DFF**	**77.8**	**176.5**	**48.57**	**37.41**

The delay is related to the speed of the signal propagation, lesser the delay faster will be the signal propagation. Rise time and fall time signifies how rapidly the logic levels of the response of the circuit changes due to change in input [24]. Table V shows that the proposed flip-flop has less delay, rise time and fall time hence it is faster than the conventional flip-flop. Also, the total delay will be the average of $t_{clk\text{-}Q}$ (LOW to HIGH) and $t_{clk\text{-}Q}$ (HIGH to LOW). Therefore, the signal propagation delay for the conventional flip-flop and proposed flip-flop are 214.9 ps and 127.15 ps respectively. The power comparison is shown in Table VI where both static power as well as dynamic power dissipation are mentioned.

TABLE VI. COMPARISON OF POWER DISSIPATION

S. No.	Design	Static Power Dissipation (nW)	Dynamic Power Dissipation (nW)	Total Power Dissipation (nW)
1.	TGDFF	10.49	1037.51	1048
2.	**Proposed DFF**	**6.79**	**180.31**	**187.1**
3.	TGDFF and MUX based Counter	58.41	4492	4550.41
4.	**Proposed Counter**	**20.55**	**1020**	**1040.55**

From Table VI we can see that the proposed flip-flop dissipates approximately five times lesser power than the conventional flip-flop and proposed counter is four times more power efficient than the conventional counter.

Now we shall look at the area requirements of the circuits on silicon chip. The layout is designed in 90 nm technology and 45 nm technology. Table VII shows the comparison of layout areas for conventional flip-flop, proposed flip-flop, conventional counter and proposed counter. From Table VII, it is clear that the proposed designs would consume less area on IC chip.

TABLE VII. LAYOUT AREA COMPARISON

S. No.	Design	Layout Area (μm^2) in 90 nm Technology	Layout Area (μm^2) in 45 nm Technology
1.	TGDFF	154.8	30.6
2.	**Proposed DFF**	**81.8**	**16.2**
3.	TGDFF and MUX based Counter	964.5	190.5
4.	**Proposed Counter**	**388.2**	**76.7**

Table VII shows that the proposed designs require nearly half of the area on IC chip as compared to existing designs. Now we shall see the device utilization of the circuits discussed so far. A CMOS circuit is a combination of PMOS and NMOS transistors hence it is necessary to know how many such transistors are required to design a specific circuit. Table VIII gives the information about device count in conventional and proposed designs.

TABLE VIII. COMPARISON OF DEVICE UTILIZATION

S. No.	Design	Total Transistors	Clock Driven Transistors	PMOS Transistors	NMOS Transistors
1.	TGDFF	24	12	12	12

2.	**Proposed DFF**	**12**	**4**	**5**	**7**
3.	TGDFF and MUX based Counter	84	12	42	42
4.	**Proposed Counter**	**40**	**4**	**17**	**23**

As we had discussed earlier, the clock driven transistors contribute the most in dynamic power dissipation. In Table VIII, we can see that in proposed circuits the clock driven transistors are less in number hence they are power efficient. Also, the switching speed of a PMOS transistor is less than an NMOS transistor due to the fact that the majority charge carriers in a PMOS transistor are holes and the mobility of holes are less than the mobility of electrons, therefore the circuits that contain more PMOS transistors suffer low switching speed. The analysis of PMOS and NMOS transistors are also given in Table VIII.

8. Conclusions and Future Scope

Here in this research work, we have designed a true single phase clock based memory element for low power applications. The circuit complexity of the proposed flip-flop is less as it requires only 12 transistors. The reduction in total power dissipation is 82.14% hence it is highly power efficient flip-flop. The signal propagation delay is 127.15 ps which is very less as compared to conventional design. Its layout area is 81.8 µm^2 and 16.2 µm^2 in 90 nm and 45 nm technology respectively. The flip-flop was configured in toggle mode in order to implement an asynchronous counter. We have proposed an UP-DOWN counter using gate diffusion input technique with the help of which a single circuit can be used as an UP counter and a DOWN counter. The proposed counter shows 77.13 % reduction in total power dissipation as compared to conventional counter. Its area requirement is 388.2 µm^2 and 76.7 µm^2 in 90 nm and 45 nm technology. The transistor utilization of the proposed counter is 40 which is nearly half of the transistors required to implement the conventional counter. Hence the proposed designs show significant reduction in power dissipation, delay, layout area and transistor count. The future aspect of this research is to design high bit counters, reduction in power dissipation by varying the power supply voltages and the proposed counter can be used to implement analog digital converters.

List of Abbreviations

In Table IX, we have listed the abbreviations used in this work.

Table IX. List of Abbreviations

Abbreviation	Description	Abbreviation	Description
ADC	Analog to Digital Converter	**MSB**	Most Significant Bit
α_k	Switching Activity at kth Node	**MUX**	Multiplexer
α_L	Switching Activity at the Load	**nm**	Nanometer
C_k	kth node Capacitance	**NMOS**	n-channel MOSFET
C_L	Load Capacitance	**nW**	Nanowatt
CLK	Clock Signal	$P_{dynamic}$	Dynamic Power Dissipation
CLK'	Complement Clock Signal	**PMOS**	p-channel MOSFET
CMOS	Complementary Metal Oxide Semiconductor	**ps**	Picosecond
D	Data or Delay	P_{static}	Static Power Dissipation
DFF	D Flip-Flop	**Q**	Output
EDA	Electronic Design Automation	**Qb (or Q')**	Inverted Output
f_{clk}	Operating Clock Frequency	**TGDFF**	Transmissio n Gate based DFF
GDI	Gate Diffusion Input	**TSPC**	True Single Phase Clock
I_{OFF_i}	Leakage Current Component when Input is Zero	**µm**	Micrometer
I_{OFF_T}	Total Leakage Current.	**VDD**	DC Voltage at Drain Terminal
LSB	Least Significant Bit	**VLSI**	Very Large Scale Integration
MHz	Megahertz	V_t	Threshold Voltage

References

[1] P. Joshi and I. Sahu, "A review paper on design of an asynchronous counter using novel reversible SG gate," in *IEEE International Conference on Innovative Mechanisms for Industry Applications, ICIMIA 2017 - Proceedings*, Jul. 2017, pp. 617–621, doi: 10.1109/ICIMIA.2017.7975535.

[2] R. Katreepalli and T. Haniotakis, "Power efficient synchronous counter design," *Comput. Electr. Eng.*, vol. 75, pp. 288–300, 2019, doi: 10.1016/j.compeleceng.2018.01.001.

[3] P. Mala S, B. S P, . A., A. Kumar, and D. Kundu, "Performance Evaluation of Ring Counter using Gated Clock," *Int. J. Eng. Technol.*, vol. 7, no. 3.12, p. 701, 2018, doi: 10.14419/ijet.v7i3.12.16458.

[4] M. Sangsefidi, D. Abedi, E. Yoosefi, and M. Karimpour, "High speed and low cost synchronous counter design in quantum-dot cellular automata," *Microelectronics J.*, vol. 73, no. November 2017, pp. 1–11, 2018, doi: 10.1016/j.mejo.2017.12.011.

[5] M. M. Abutaleb, "Robust and efficient quantum-dot cellular automata synchronous counters," *Microelectronics J.*, vol. 61, no. December 2016, pp. 6–14, 2017, doi: 10.1016/j.mejo.2016.12.013.

[6] K. S. Bhavani and V. Alinvinisha, "Utilization of QCA based T flip flop to design counters," *ICIIECS 2015 - 2015 IEEE Int. Conf. Innov. Information, Embed. Commun. Syst.*, 2015, doi: 10.1109/ICIIECS.2015.7193059.

[7] D. Liu and C. Svensson, "Power Consumption Estimation," *October*, vol. 29, no. 6, 1994.

[8] F. N. Najm, "A Survey of Power Estimation Techniques in VLSI Circuits," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 2, no. 4, pp. 446–455, 1994, doi: 10.1109/92.335013.

[9] M. Pedram, "Tutorial and Survey Paper Power Minimization in IC Design : Principles and Applications," *Design*, vol. 1, no. 1, pp. 3–56, 1996.

[10] R. Turaka and D. S. S. Ram M., "Low power VLSI implementation of real fast Fourier transform with DRAM-VM-CLA," *Microprocess. Microsyst.*, vol. 69, pp. 92–100, 2019, doi: 10.1016/j.micpro.2019.05.016.

[11] A. Jamal, J. P. Prasad, and P. G. Student, "Design of Low Power Counters Using Reversible Logic," *Int. J. Innov. Res. Sci. Eng. Technol. (An ISO*, vol. 3297, no. 5, pp. 2319–8753, 2007.

[12] H. Jianping, C. Lizhang, and L. Xiao, "A new type of low-power adiabatic circuit with complementary pass-transistor logic," *IEEE Int. Symp. Semicond. Manuf. Conf. Proc.*, vol. 2, pp. 1235–1238, 2003, doi: 10.1109/ICASIC.2003.1277438.

[13] D. Soni and M. V Shah, "Review on Modified Gate Diffusion Input Technique," *Int. Res. J. Eng. Technol.*, vol. 4, no. 4, pp. 874–878, 2017, [Online]. Available: https://www.irjet.net/archives/V4/i4/IRJET-V4I4178.pdf.

[14] G. R. Mahendra Babu and S. Bhavani, "Primitive cells using gate diffusion input technique: A low power approach," *Int. J. Recent Technol. Eng.*, vol. 8, no. 1, pp. 257–260, 2019.

[15] V. Vaishali, S. Rajarajeshwari, and S. Chandrasekaran, "A STUDY ON LOW POWER IMPLEMENTATION OF MULTIPLEXER," *Int. J. Emerg. Technol. Comput. Sci. Electron.*, vol. 25, no. 5, 2018.

[16] K. Rahbari and S. A. Hosseini, "Novel ternary D-Flip-Flap-Flop and counter based on successor and predecessor in nanotechnology," *AEU - Int. J. Electron. Commun.*, vol. 109, pp. 107–120, 2019, doi: 10.1016/j.aeue.2019.07.008.

[17] M. Prithivi Raj and G. Kavithaa, "Dynamic signal driving strategy based high speed and low powered dual edge triggered flip flop design used memory applications," *Microprocess. Microsyst.*, vol. 71, 2019, doi: 10.1016/j.micpro.2019.102879.

[18] A. Saha, R. Pal, A. G. Naik, and D. Pal, "Novel CMOS multi-bit counter for speed-power optimization in multiplier design," *AEU - Int. J. Electron. Commun.*, vol. 95, pp. 189–198, 2018, doi: 10.1016/j.aeue.2018.08.015.

[19] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd Editio. Pearson, 2003.

[20] G. B. Hamad, S. R. Hasan, O. A. Mohamed, and Y. Savaria, "New insights into the single event transient propagation through static and TSPC Logic," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1618–1627, 2014, doi: 10.1109/TNS.2014.2305434.

[21] N. Kawai *et al.*, "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," in *Proceedings of the 2013 IEEE Asian Solid-State Circuits Conference, A-SSCC 2013*, 2013, pp. 117–120, doi: 10.1109/ASSCC.2013.6690996.

[22] J. F. Lin, M. H. Sheu, Y. T. Hwang, C. S. Wong, and M. Y. Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 25, no. 11, pp. 3033–3044, 2017, doi: 10.1109/TVLSI.2017.2729884.

[23] Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmierski, "Ultra-low power 18-transistor fully static contention-free single-phase clocked flip-flop in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 550–559, 2019, doi: 10.1109/JSSC.2018.2875089.

[24] S. Bhunia and M. Tehranipoor, "A Quick Overview of Electronic Hardware," *Hardw. Secur.*, pp. 23–45, 2019, doi: 10.1016/b978-0-12-812477-2.00007-1.

Jitesh Singh Chauhan did his B. Tech in Electronics and Communication Engineering (2017) from Dr. A.P.J. Abdul Kalam Technical University, Lucknow, India. He is pursuing M. Tech in Microelectronics from Institute of Engineering and Technology, Lucknow. His research interests include low power VLSI designing and enhancing the performance of digital systems.

Ram Chandra Singh Chauhan is currently working as Associate Professor in department of Electronics and Communication Engineering at Institute of Engineering and Technology, Lucknow, India. He received his Ph.D. from AKTU Lucknow (ECE – HBTI Kanpur). He received his M. Tech in ECE-Digital system from MNNIT Allahabad. His research interest includes VLSI designing, Coding Theory, Optical Switching, Optical Multiple Access Schemes, Optical Networking, Formation of clique groups and their applications in social networking, Hybrid Networks, etc.