International Journal of Computing and Digital Systems
ISSN (2210-142X)
Int. J. Com. Dig. Sys. 11, No.1 (Mar-2022)

https://dx.doi.org/10.12785/ijcds/110182

Performance and Area Optimization of SRAM Cell in Nanocomputing Application

Anurag Yadav[1] **and Subodh Wairya**[2]

[1]*Department of Electronics and Communication Engineering, Institute of Engineering and Technology, Lucknow, India*
[2]*Department of Electronics and Communication Engineering, Institute of Engineering and Technology, Lucknow, India*

Received 19 Mar. 2021, Revised 2 Feb. 2022, Accepted 9 Mar. 2022, Published 31 Mar. 2022

Abstract: A Shrink in technology leads to decrease in voltage supply which returns in power leakage. This affects the data stability in Static Ram Access Memory (SRAM) cell. Static noise margin (SNM) is needed for the measurement of data stability in SRAM cell. Data stability for SRAM cell relies on the largest DC noise which can be ignored at the inverters outputs which are cross coupled without changing the data in SRAM cell. This paper presents 6T, 7T, 8T, 9T, 10T design and analysis which increases the data stability of SRAM during write and read mode. These cells are compared with respect to their read static noise margin (RSNM), hold noise margin (HSNM), write 0 delay, write 1 delay, average write delay, static power, average dynamic power, total power dissipation and surface area. Finger method is used to create layouts of different SRAM cells which reduce the surface area of cell. This method is also required to reduce the parasitic in layout design. The layout of different cells of SRAM and an SRAM with 4×4 array of 6T cell is implemented on virtuoso tool of cadence software using 45nm Technology. After the simulation outcome, it is found that 10T cell has maximum RSNM which is 0.42V and it has minimum total power dissipation. Process variation and Monte Carlo simulation for different SRAM cells are carried out. Process variation is done for the RSNM parameter of the memory cells. After the simulation it is observed that the performance of 10T design is best among all simulated SRAM cells. Comparison of 6T, 8T and 9T cell design with previous work shows the improvement in RSNM at the price of write delay. 10T SRAM cell using CNFET (carbon nanotube field-effect transistor) is simulated which has channel length of 11nm at 0.3V of voltage supply. After simulation it has observed that 10T SRAM cell based on CNFET has low total power of dissipation.

Keywords: SRAM cell, RSNM, HSNM, Power dissipation, Write delay, Corner analysis

1. INTRODUCTION

The requirement of SRAM is increasing with every passing day. This is mainly due to the requirement of handheld, compact devices such as mobiles and minicomputers. These devices have high speed microprocessors. Cache memory is used in the microprocessor to access data faster. To improve the speed and functioning, the Static Random Access Memory is required to work as cache memories[1], [2], [3]. SRAM also fulfills the need of battery operated devices like wireless sensor and biomedical devices where the lifetime of battery and power consumption is a very important criterion. Many smart devices are multifunctional and require less power dissipation [4], [5], [6], [7], [8]. In very large scale integration (VLSI), thousands of transistors are fit together on a one chip which has small surface area [9]. Low power in portable devices becomes a primary factor [10]. Many SRAM cells are used to design an array of SRAM cells to load huge amount of data. Memory covers a large area of the system on chip. Due to this scaling of transistor dimensions is the need of new technology. It helps in reducing the area of cell which results in reduction of size of SRAM and improves integration density, but it increases leakage current [11], [12], [13], [14], [15], [16]. Each cell has a problem of leakage. SRAM array, which consist of many cells, becomes a big source of leakage current. Problem of data stability in SRAM cell arises due to voltage scaling and device dimension in new technology generation [17], [18], [19].

Data durability of the cell in hold mode and read mode is the main restriction in advanced technology [20]. The RSNM is SNM at the read mode is deteriorated due to mismatch in transistor and reduction in voltage supply. This problem can be resolved by using separate read circuit [21]. This read circuit increases the quantity of transistors in the cell which causes in an increase in domain of SRAM cell. During read mode existing data in the cell is read out using sense amplifier. There are some methods through which data stability can improve during read and write mode of operation. To improve SNM and reduction in area of SRAM, different SRAM cells are designed [1]. The SRAM cell's SNM value can also be enhanced by proper sizing the

E-mail address: anuraglko2014@gmail.com, swairya@gmail.com

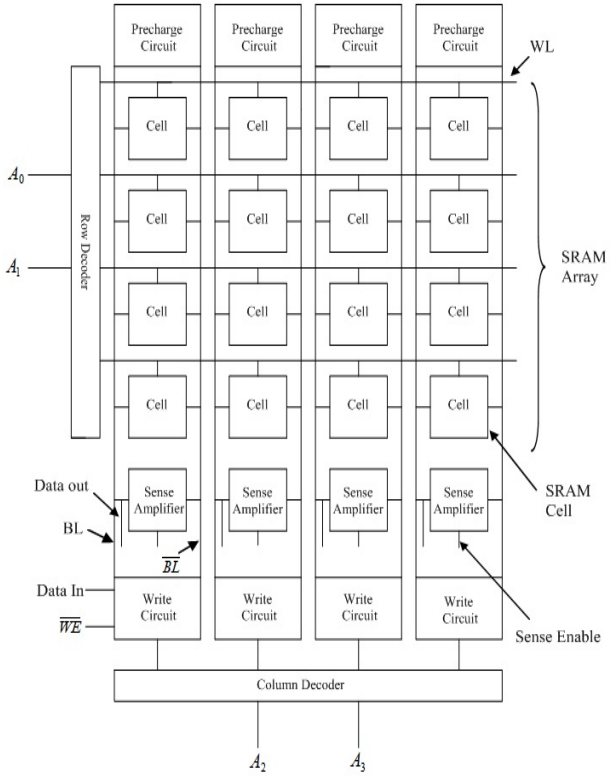

Figure 1. Block diagram of SRAM Architecture [4]

ratio of transistor [22]. Proper sizing of transistor improves data stability in both read and write deed [4], [23], [24]. Read-write circuit is required in memory design which can change the data on memory array at the time of write process and retain data in read process. SRAM is static because of that it maintains its data as the power supply is applied without needing periodic refreshment [23], [25].

Fig.1 depicts the SRAM architecture's bock diagram for 4×4 SRAM array which consists of array of cell, bit line BL and bit bar line $\overline{BL}$, word line WL, sense amplifier, sense enable, pre-charge circuit, row decoder, column decoder, write enable $\overline{WL}$, data input and data out. Row and column decoder are used here to select any one memory element in array where write or read action has to be performed. Read operation is performed when $\overline{WL}$ write enable is 1 and write action is performed when write enable is 0 using proper control at BL and $\overline{BL}$. Sense enable is employ to enable sense amplifier during read mode.

The scaling of transistors is the key for the semiconductor industry which indicates great increments in computing energy and power efficiency. Along with the advancements in silicon-based electronics, many alternative technologies are being developed at the same time. Hence, carbon nanotubes (CNTs) are fulfilling the existing demand of semiconductor technologies [26]. Single-walled carbon nanotubes are implemented in VLSI because of their mechanical flexibility/stretchability, extraordinary charge carrier mobilities, and solution processing. In particular, semiconducting single walled nanotubes (SWNTs) have surfaced as a great material for a range of electronic applications, starting from logic circuits, field-effect transistors and chemical and biological sensors to optoelectronic devices, electronic skins, and computers [27]. Electronic devices made from CNFETs offer high energy efficiency [28], [29]. Additionally, CNFET CMOS process are designed to be tunable (e.g., control CNFETs threshold voltage), robust (e.g., air-stable) and silicon CMOS simpatico (to be integrated within current manufacturing process) [28]. However, silicon CMOS suitable with CNT doping to design NMOS CNFETs do not exist. Since there are several issues related to performance advantages in silicon-based computing systems, some alternative technologies are being considered. In nanotechnology CNT is universally accepted nanotechnology to design digital circuits. CNFETs are used due to its low Energy-Delay-Product (EDP) for digital systems. Such EDP benefits can also be used for yielding cooling benefits for 3D ICs [30]. SRAM can also be implemented using CNFET; it has low leakage power and EDP.

In this work performance analysis and simulation of 6T, 7T, 8T, 9T and 10T SRAM cells are carried out on virtuoso tool of cadence software using 45nm technology at 1V supply voltage. The comparison of these cells is done by their respective RSNM, HSNM, write 0 delay, write 1 delay, average write delay, power dissipation and surface area. CNFET based 10T SRAM Cell is simulated at 0.3V supply voltage which has 11nm channel length. In section II different SRAM cell designs are explained with their transient simulation, RSNM and HSNM simulation. Section III explained the layout of different SRAM cell design. Section IV describes the layout of SRAM with 4×4 array of 6T cell. In Section V, the analysis of simulation results and their comparison is shown. Section VI extracts the conclusion.

2. DIFFERENT SRAM CELL

A. 6T SRAM Cell

This cell contains 6 transistors, out of which two are PMOS and four are NMOS as shown in fig. 2 [20], [22], [31], [32]. In this circuit there are two CMOS based inverters both are cross connected to each other with access transistors NM3, NM4. Data is stored in internal node P, Q through these access transistors.

The action of memory cell is divided in three parts-hold mode, write mode and read mode. These actions are understood with the circuit of 6T memory cell as represents in fig. 2.

In hold mode, word line (WL) is not active, so the access transistors are disabled which remove the connection from BL and BLB to the internal mode of the cell. There is no

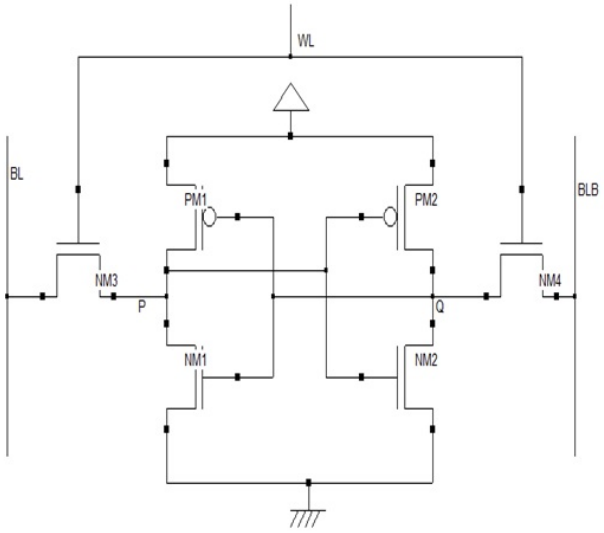

Figure 2. 6T SRAM Cell's schematic [20],[22],[31],[32]

change in the data stored at inner node P and Q until the voltage supply is active. In the write operation, consider the case when 1 is at P and 0 is at Q node. Firstly precharged the BL and BLB at this time WL is not active. After precharged the BL and BLB, activate WL. To write 0 at the node P where 1 is already stored, bit line BL of that side make low using external circuit during this time BLB is remain at pre-charged. So there is discharging current from BLB to Q. on the other side, there is a potential difference between BL and P node through access transistor NM3. There is a discharging path available from P to BL. Discharging current starts flowing from node P to BL due to which the voltage of node P starts decreasing. When the potential at P node reduces below the threshold voltage of NM2, NM2 turns off and the PM2 turns ON due to this discharging at node Q and BLB gets stop. PM2 turns ON, which pulls the voltage at Q to 1. At this time the data at P comes to 0 and Q gets modified with 1 [23].

In the read mode, if 1 is at P and 0 is at Q node, firstly precharged BL and BLB at this time WL is not active. Then activate the WL, there is no potential difference between P and BLB, no current is there. On the other side, there is a potential difference between BLB and Q. Discharging current starts flowing, it reduces the voltage level of BLB. The difference in BL and BLB is sensed with sense amplifier which estimates that 1 is stored at P node. During the discharge of BLB to Q through access transistor NM4, there is a chance of bump up in voltage at Q. So this increases the chances of tripping the inverter which is at P side. This can modify the stored data at P and Q of the cell. To enhance the read assurance the width of NM1, NM2 which are the pull down transistors should be greater than NM3, NM4 access transistors. In the write mode, stability can improve by increasing the width of access transistor NM3, NM4 as compared to pull up transistors PM1 and PM2 [31], [33]. Simulation of 6T memory cell is illustrated in fig.3, which shows the write and hold state of memory cell.

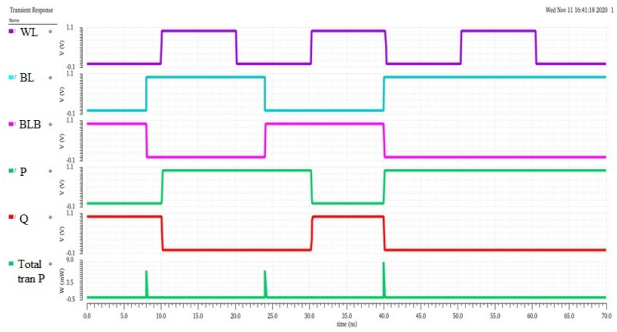

Figure 3. Simulation waveform of 6T Cell

SNM's simulation for 6T cell during read mode and hold process is represented in fig.4 the HSNM of 6T cell is 0.41 V and RSNM of the 6T cell is 0.21 V. RSNM is nearly half of HSNM. There is problem of data stability during read mode. SNM value is calculated with the help of side of square in butterfly curve. Butterfly curve is obtained with the DC simulation of both the inverters in the cell. SNM of an SRAM cell is equal to minimum of SNM1, SNM0 [34].

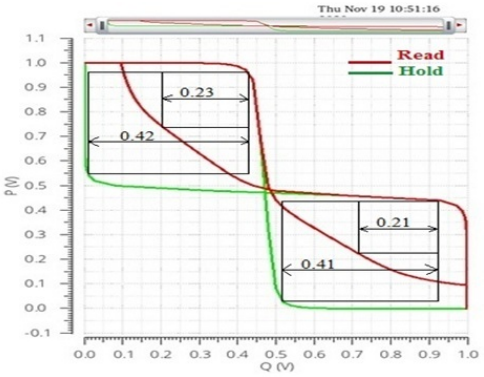

Figure 4. Simulation waveform for RSNM of 6T Cell

B. 7T SRAM Cell

It has one additional transistor comparison of 6T memory cell. It consists of 5 NMOS and 2 PMOS transistors as presented in fig.5 [1], [35]. This extra transistor NM5 keep in series with pull down transistor NM1 to improve the data retention during read mode.

During hold action, the WWL and WL are disabled and WLB is active. In the write mode WWL and WL are active and WLB is off, process remains equivalent with 6T SRAM cell. In read process, WL is activated, WWL and WLB are deactivated. Read operation is single sided in 7T SRAM cell. BLB is precharged at supply voltage first, then activates WL according to the data retained at Q there is discharging

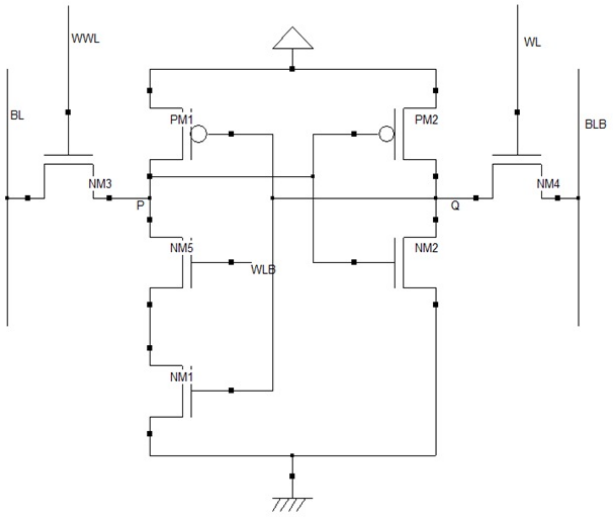

Figure 5. 7T SRAM Cell's schematic[1], [35]

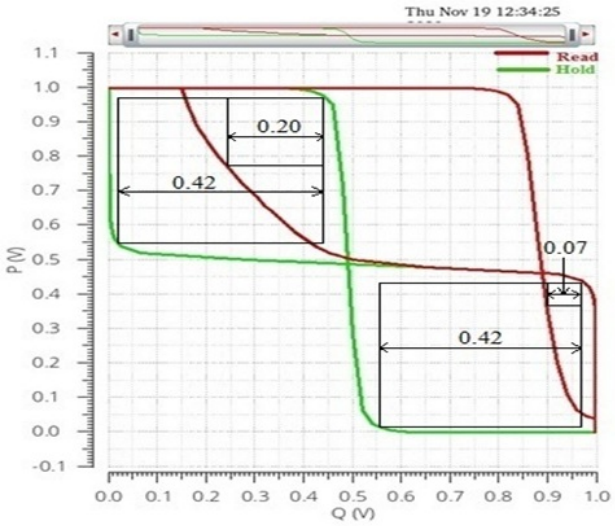

Figure 7. Simulation waveform for RSNM of 7T Cell

current through access from BLB to NM2 though access transistor NM4. Voltage level of BLB is sensed with sense amplifier. Sense amplifier estimates the data stored at P and Q. Extra transistor NM5 is off in read and write process, it is for the data durability in the cell. Simulation of 7T memory cell is depicted in fig.6.

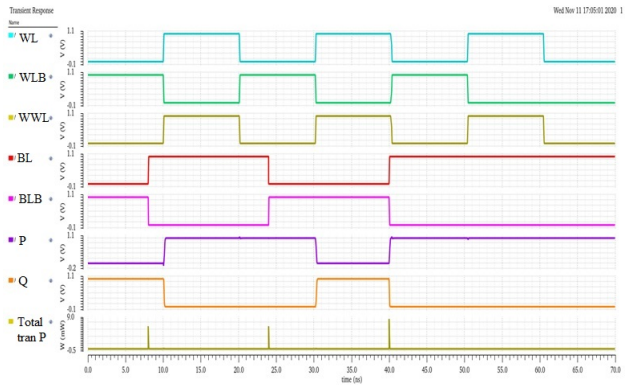

Figure 6. Simulation waveform of 7T Cell

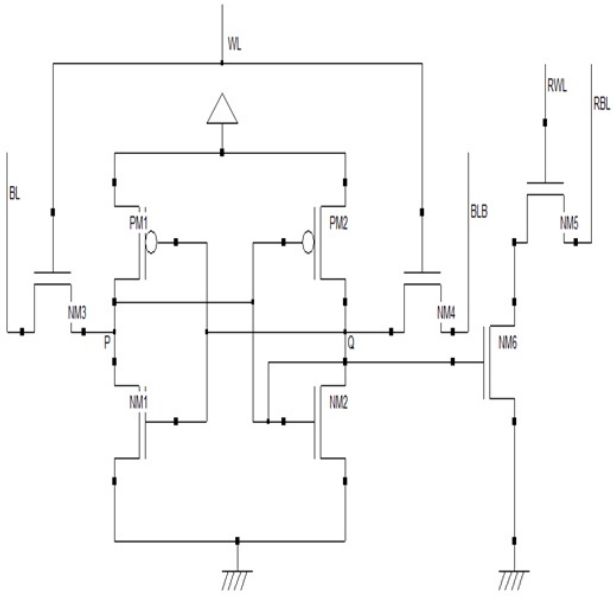

Figure 8. 8T SRAM cell's schematic [1]

Waveform in fig.7 illustrates the SNM for 7T SRAM cell in the read and hold process. RSNM is 0.07 V and HSNM is 0.42 V for 7T SRAM cell. The RSNM value is very less to retain data in read mode. It also requires NM5 with large width, this result in enhanced in surface area.

C. 8T SRAM Cell

This design has total 8 transistors which are depicted in fig.8 [1]. The requirement of read durability in 6T SRAM cell is enhanced with one separate read circuit which has two NMOS transistors NM5, NM6 [36]. The internal node is totally isolated from read circuit, so data at internal nodes P and Q are stabilized [1], [37].

In write mode, read word line (RWL) is deactivated and write action is remaining same as 6T memory cell. In read mode, WL is deactivated and precharged the read bit line (RBL) then activates the RWL. The internal node P is connected to the gate of NM6. If data at P is 1, then NM6 is turned ON. There is a close path from RBL to ground through access transistor NM5 and NM6. Discharging current start flowing and voltage level of RBL starts reducing. If data is 0 at P then NM6 is turned OFF and circuit is open. There is no current and voltage level at RBL remains high. Change in voltage level of RBL is sensed

by sense amplifier and estimates the data at the internal node. Simulation of 8T memory cell is depicted in fig.9. Simulation of SNM for 8T SRAM Cell in read process is depicted in fig.10. The RSNM and HSNM values are same, which is 0.41V. It means data stability is getting improved in this design.

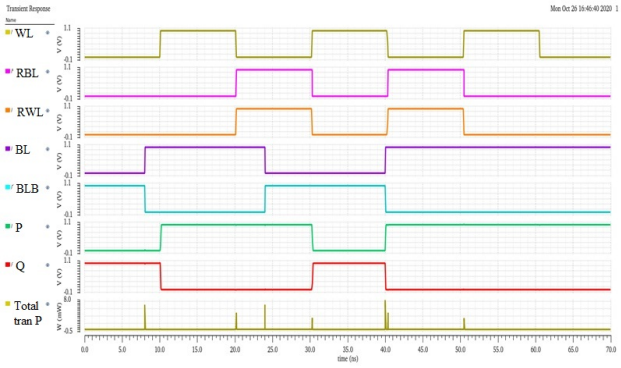

Figure 9. Simulation waveform of 8T Cell

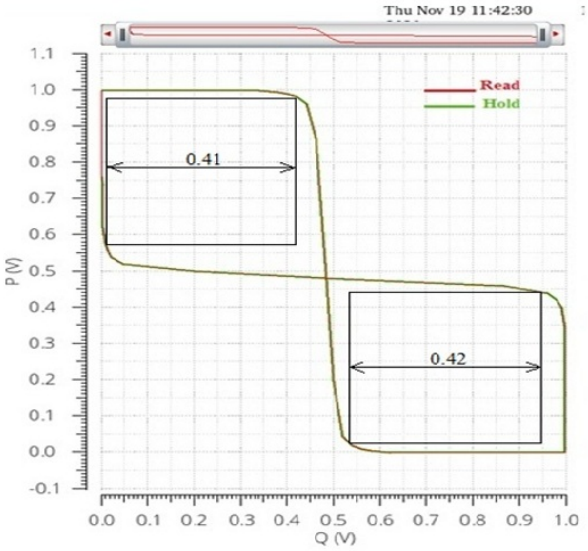

Figure 10. Simulation waveform for RSNM of 8T Cell

D. 9T SRAM Cell

In this design, there are three additional NMOS transistors as compared to 6T memory cell. There are 7 NMOS transistors and 2 PMOS transistors. During read operation, data at internal node is completely separated from BL and BLB. This improves the RSNM. Schematic of 9T cell which is illustrated in fig.11 [17], [38]. Schematic consist of two inverters are cross connected and then joined with two pass transistors NM3, NM4 and three transistors NM5, NM6, NM7 as read circuit. Internal node of cell P and Q are attached to the gate of two read NM5 and NM6. NM5 and NM6 are read access transistors. During standby and write

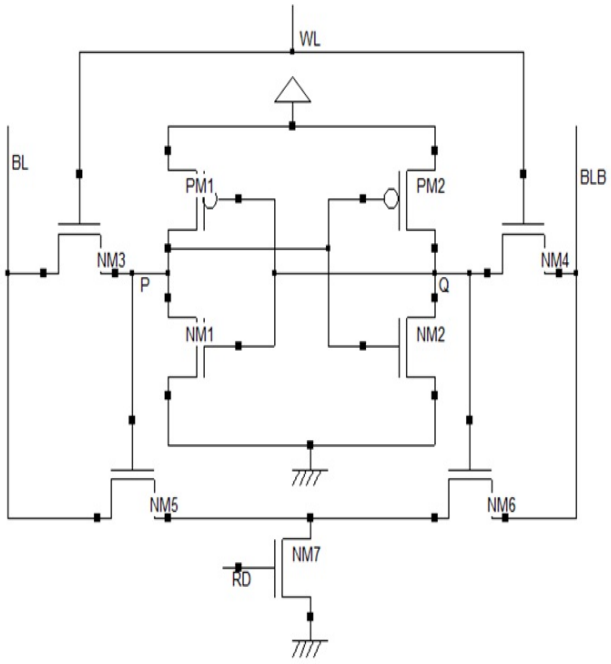

Figure 11. 9T SRAM cell's schematic [17], [38]

mode read signal RD at NM7 is 0. Standby and read mode operation remain similar to operation in 6T memory cell.

In read operation, WL is deactivated and BLB and BL precharged to supply voltage that activate read signal RD as 1. If data at P is 1, this turns ON read access transistor NM5 and BL starts discharging through read access transistor NM5 and NM7. On the other side data at Q is 0, NM6 is OFF and BLB remains high [17]. This difference of voltages between BLB and BL is being taken by sense amplifier and estimated the data at the internal node. Simulation of 9T cell is depicted in fig.12.

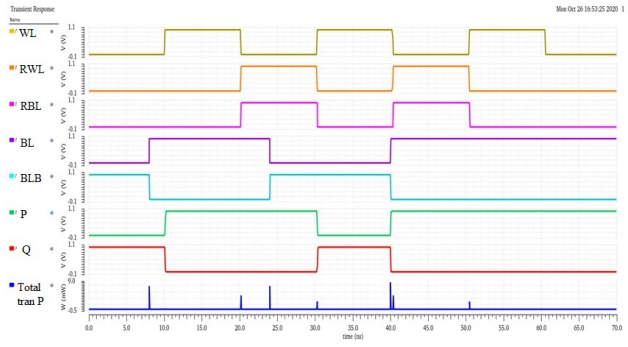

Figure 12. Simulation waveform of 9T SRAM Cell

The RSNM and HSNM values are same, which is 0.41V. It means data stability is getting improved in this design. Simulation for RSNM of 9T cell is depicted in fig.13.

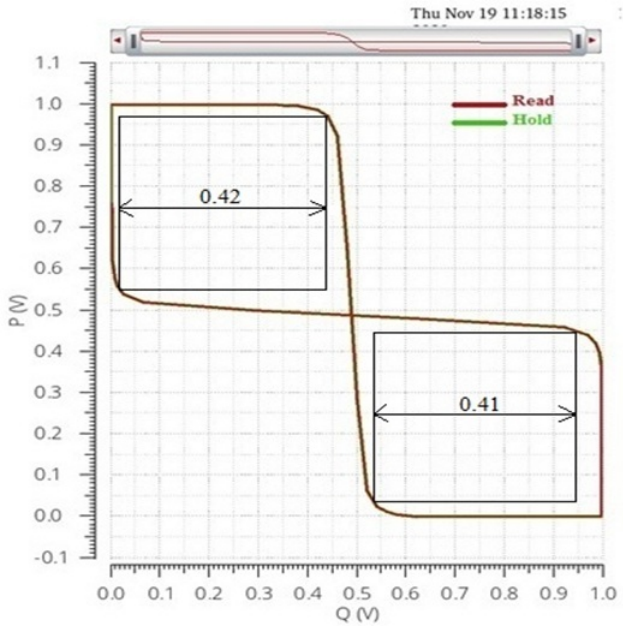

Figure 13. Simulation waveform for RSNM of 9T SRAM Cell

E. 10T SRAM Cell

This design has 2 more transistors as compared to 8T memory cell as depicted in fig. 14 [39], [40]. 8T SRAM cell has the problem of leakage current in read process when read word line (RWL) is deactivated. To reduce this problem, two additional transistors PM3 and NM7 are used in the read circuit.

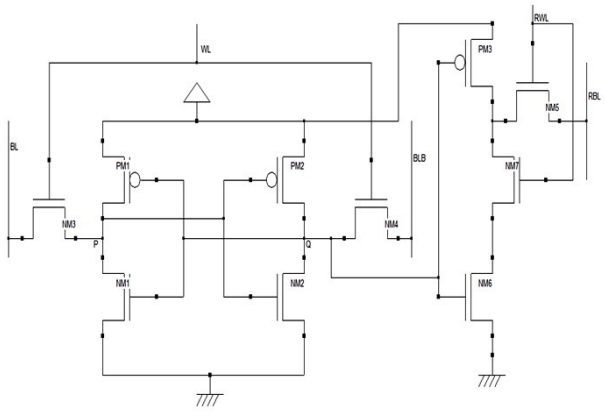

Figure 14. 10T SRAM Cell's schematic [39], [40]

Write mode is similar as 6T memory, WL is activated and RWL is deactivated in this mode. In read mode, WL is deactivated; pre-charge the read bit line RBL to voltage supply level then activates the RWL. Read operation is same as 8T memory cell. Simulation of 10T memory cell is depicted in fig.15.

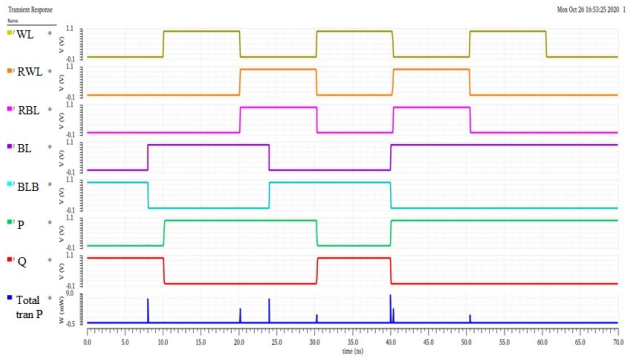

Figure 15. Simulation waveform of 10T SRAM Cell

The RSNM and HSNM values are same, 0.42V. It means data stability is getting improved in this design. Simulation is depicted in fig.16. The butterfly curve is totally symmetric in this design both windows are equal size.

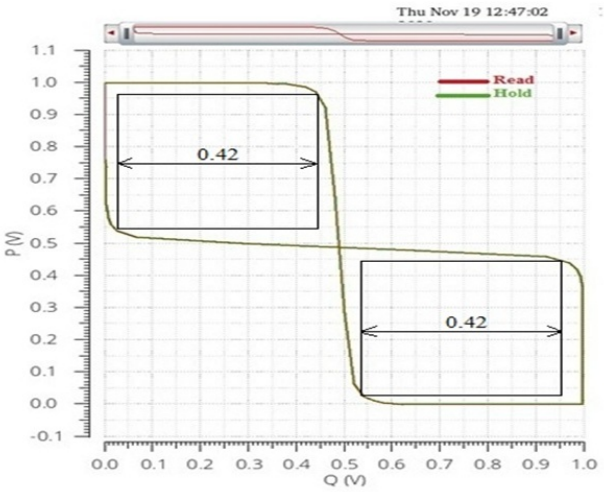

Figure 16. Simulation for RSNM of 10T SRAM Cell

F. CNFET BASED 10T SRAM Cell

CNFET based CMOS has channel length 11nm. Supply voltage scales down to 0.3V. This CNFET CMOS design 10T SRAM Cell has total 10 CNFET based transistors as depicted in fig.17 [39], [40].

Fig.18. illustrates the simulation of this 10T SRAM Cell. This simulation depicts the write and hold operation. During the read, RBL is high. At this time, there is no change in data at the internal node of SRAM cell. The operation of CNFET used 10T Cell is identical as MOSFET used10T Cell for memory.

3. LAYOUT OF DIFFERENT SRAM CELL

The surface area calculation is done for 6T, 7T, 8T, 9T and 10T cells with 45nm technology. Finger method is used to reduce the surface area and parasitic of the layout. This

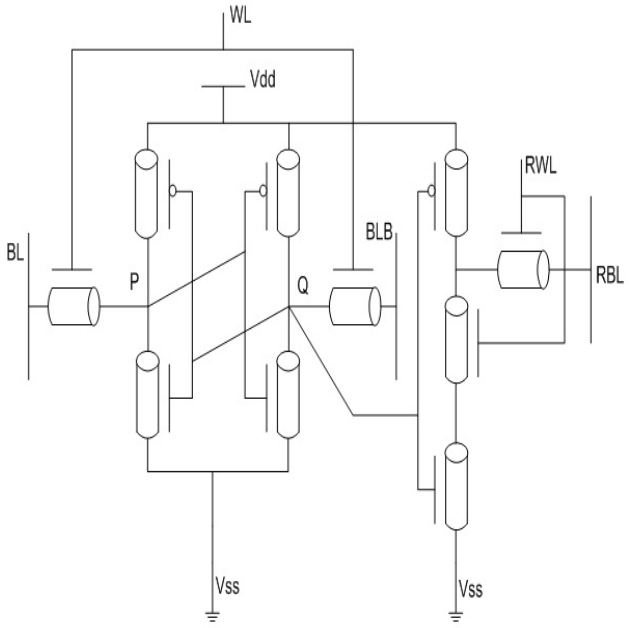

Figure 17. CNFET based 10T SRAM Cell's schematic [39], [40]

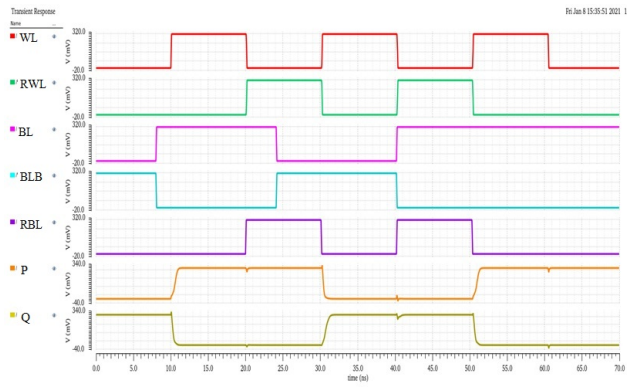

Figure 18. Simulation waveform of CNFET based 10T SRAM Cell

layout is created with reduced transistor width. The layout of 6T memory cell is illustrated in fig.19. 6T cell's layout has width 3.27 μm, height 3.04 μm and surface area 9.93 μm^2.

Layout of 7T memory cell is depicted in fig.20. 7T cell's layout has width 3.8 μm, height 3.83 μm and surface area 14.54 μm^2 . The surface area of 7T cell is increased due to the size of NM5 transistor to find data stability in read mode. RSNM value is very less in this design which is 0.07V. Finger method helps make this layout compact; otherwise the surface area will increase more than 14.54 μm^2 .

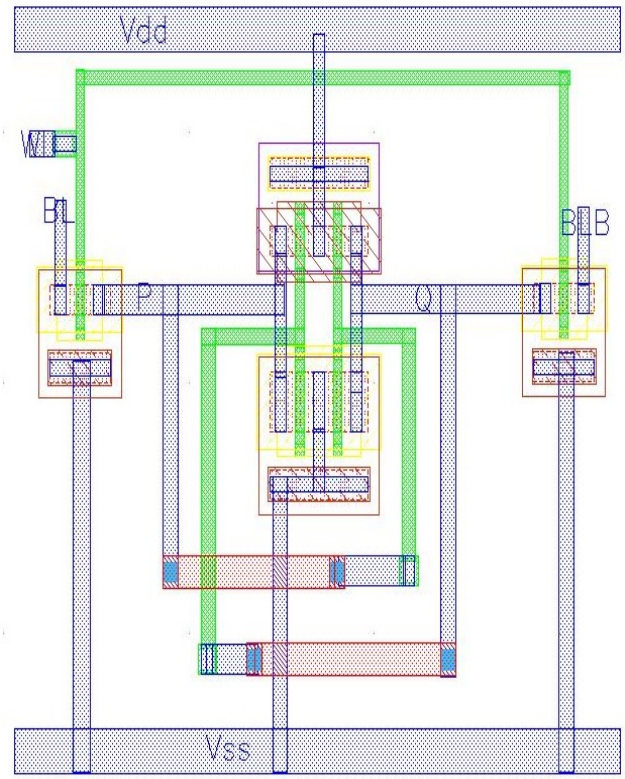

Figure 19. Layout of 6T Cell

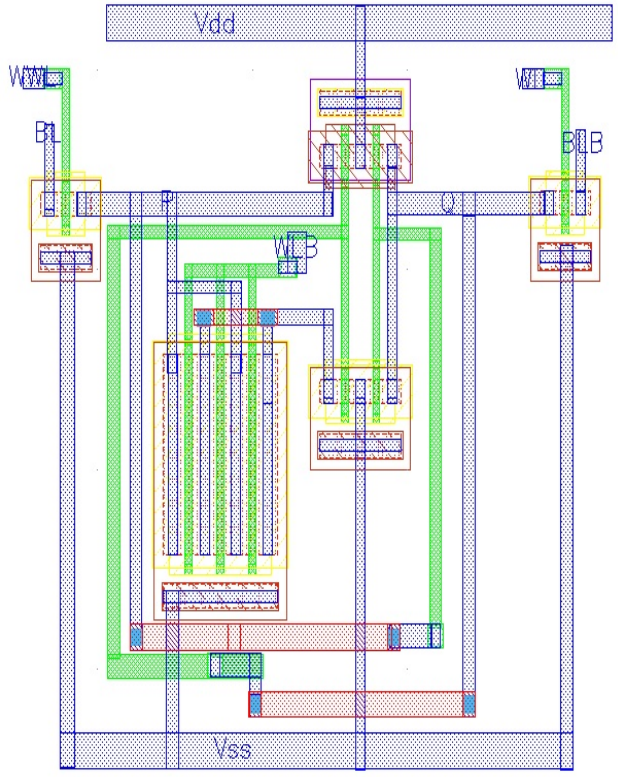

Figure 20. Layout of 7T Cell

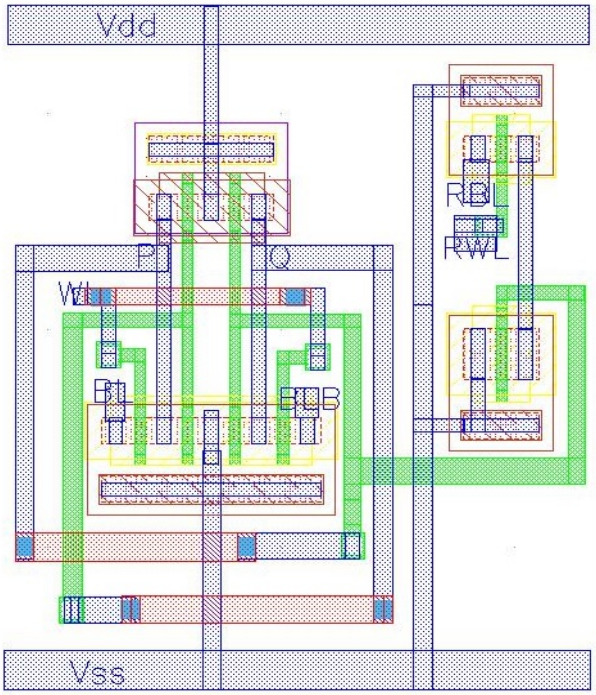

Figure 21. Layout of 8T Cell

Layout of 8T memory cell is depicted in fig.21. 8T cell's layout has width 2.54 μm, height 3.17 μm and surface area 8.07 μm^2. 9T cell's layout is depicted in fig.22.

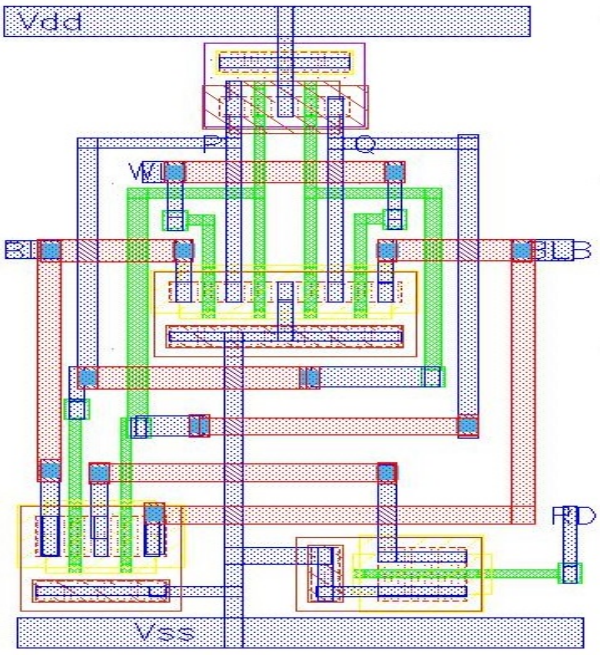

Figure 22. Layout of 9T Cell

9T memory cell's layout has width 2.35 μm, height 3.92 μm and surface area 9.18 μm^2.

Fig.23 depicts the 10T memory cell' layout. 10T cell's layout has width 3.37 μm, height 3.06 μm and surface area 10.30 μm^2.

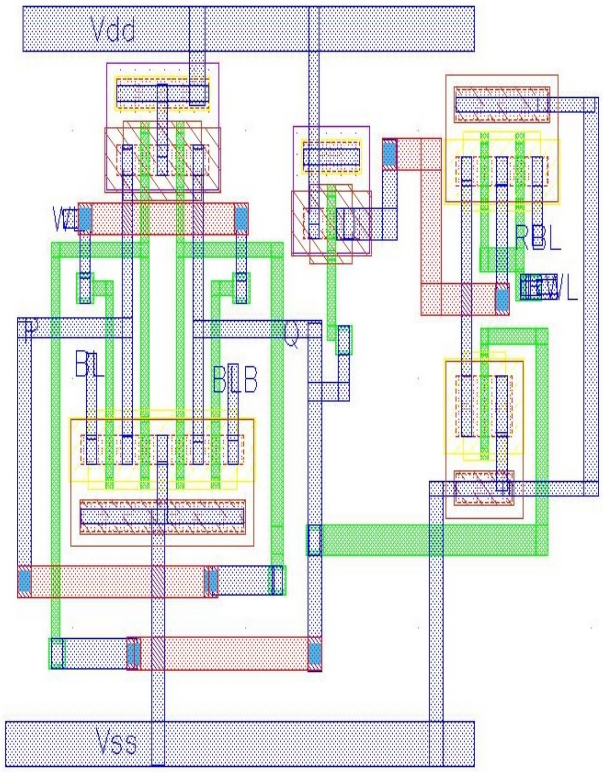

Figure 23. Layout of 10T Cell

4. SRAM WITH 4×4 ARRAY OF 6T SRAM CELL

A 4×4 array of SRAM using 6T memory cell is illustrated in fig.24. This array has width 18.2 µm and height of 16.25 µm. Surface area of the 4×4 array of SRAM is 295.75 μm^2. This memory is created with the help of 6T SRAM cell. Total 16 memory cells are used in this design. Technology used to create this layout is 45nm. Fig.25 depicts the simulation of 4×4 array with 6T SRAM Cell. In this simulation data write operation is perform in column 0 of the array. BL0 and BLB0 are the bit lines for column 0. The role of WL is to select row 0-3 in array. P and Q are the internal nodes of the 6T SRAM cell. P00,Q00 for row 0 and column 0, P10,Q10 for row 1 and column 0, P20,Q20 for row 2 and column 0, P30,Q30 for row 3 and column 0. The static power of this array in simulation is depicted in fig.25 is 23.14μW, average dynamic power is 3.47μW and total power dissipation is 26.61μW.

The layout of SRAM which has 4×4 array of 6T SRAM Cell, row decoder, column decoder, sense amplifier, precharge circuit, is depicted in fig.26. Memory Cell is selected

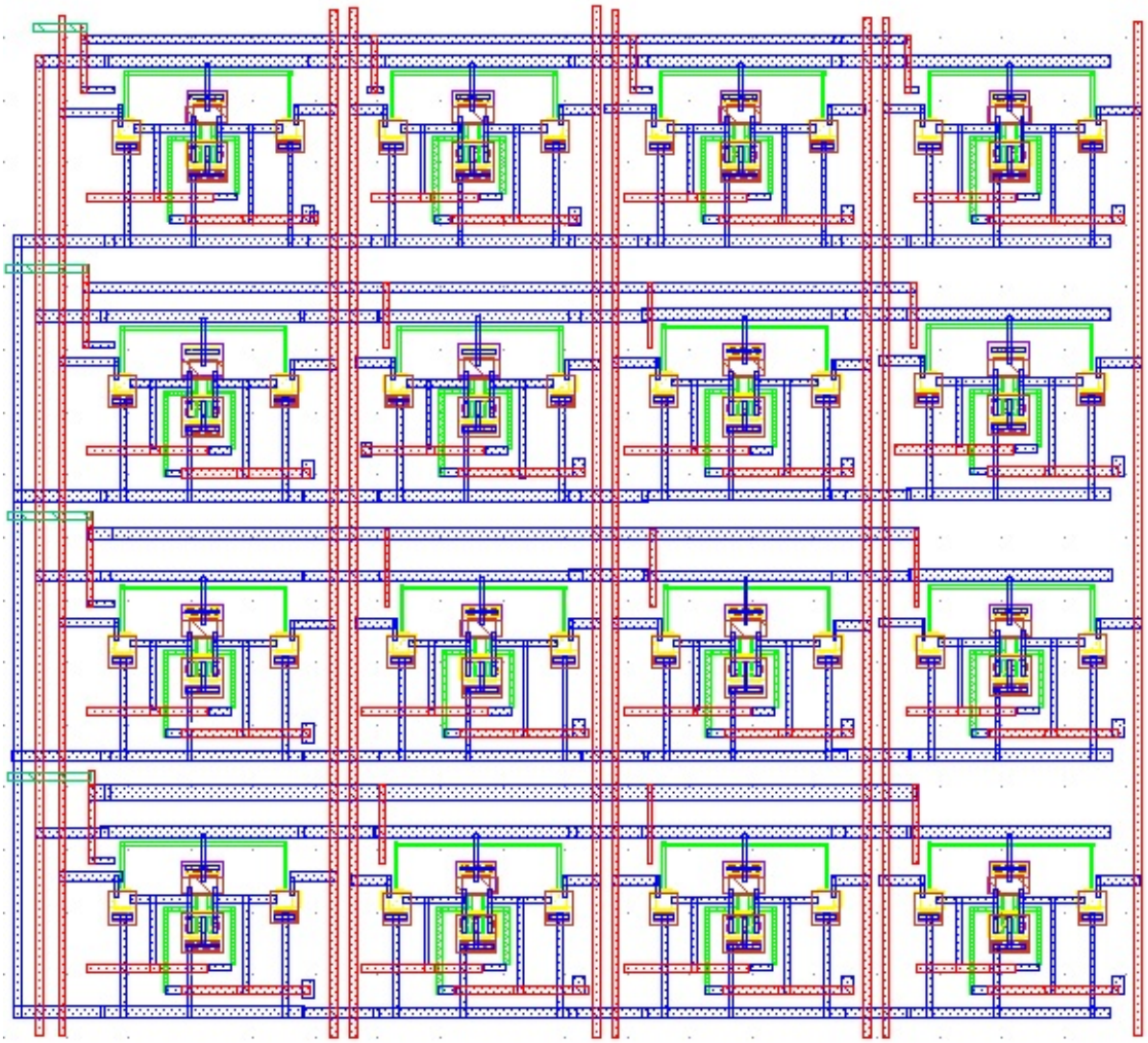

Figure 24. Layout for 4×4 array using 6T SRAM Cell

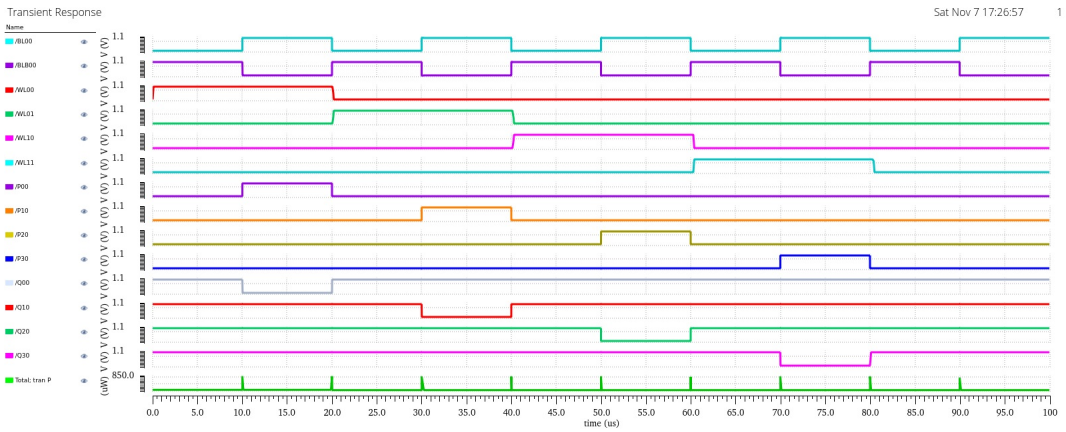

Figure 25. Transient waveform of 4×4 array with 6T SRAM Cell

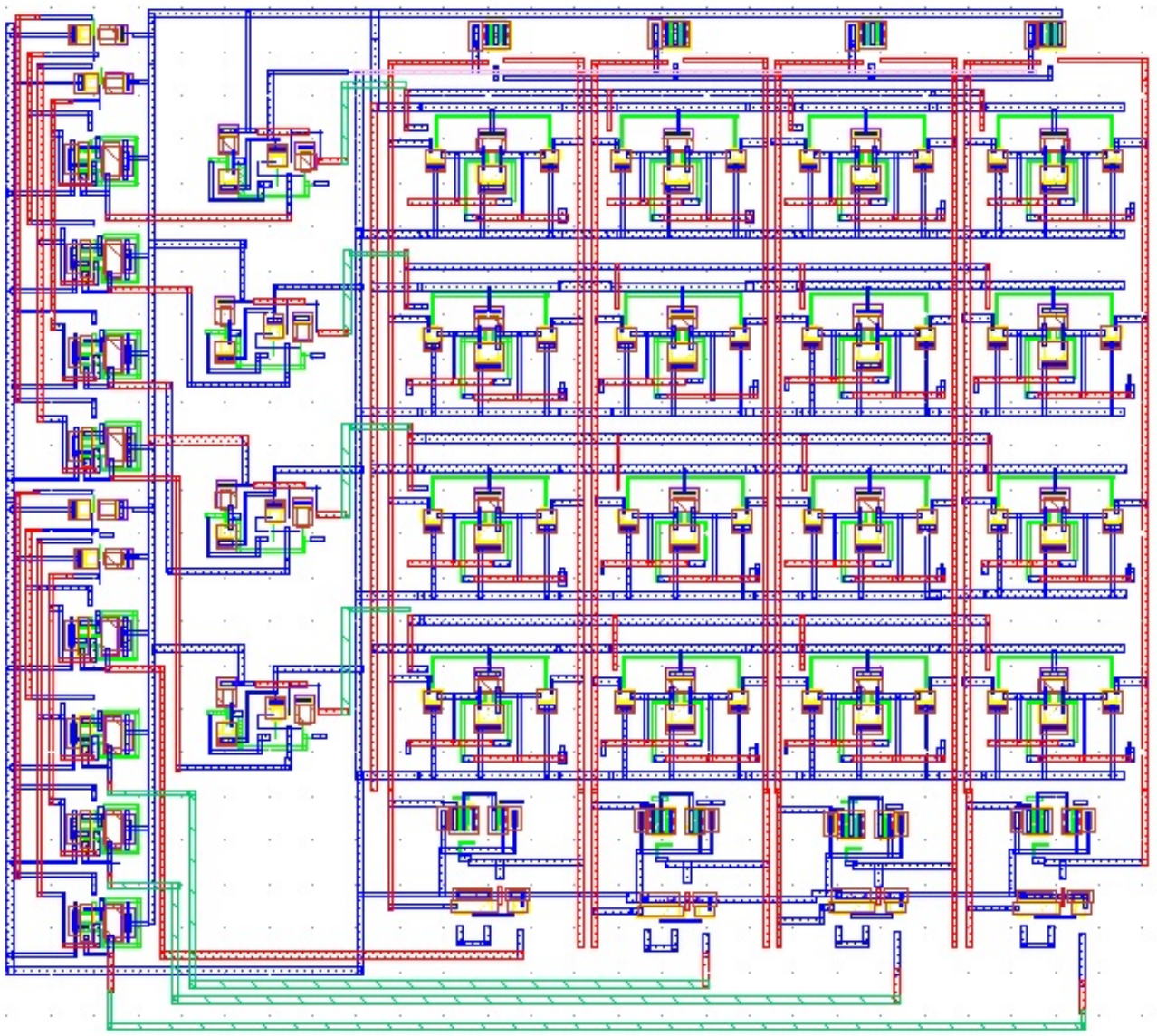

Figure 26. Layout for SRAM with 4×4 ARRAY of 6T Cell

from array to perform read and write operation using decoder circuits. There is read-write circuit for selecting read and write operation. Sense amplifier is used to sense the data at the internal node of the cell at the read time. Pre-charged circuit is at the top of array. The circuits which are at the bottom are sense amplifier and read-write circuit. This layout has width 26.095 µm, height 23.26 µm and surface area 606.84 μm^2.

5. RESULT AND DISCUSSION

Observation of different parameters for 6T, 7T, 8T, 9T and 10T cell designs of SRAM is presented in table I. These parameters are RSNM, HSNM, write delay, power dissipation, width, height and surface area. These parameters are simulated using 45nm technology with 1V supply voltage at 27ºC. Virtuoso tool of cadence software is used for the simualtion and creating layout. All results are taken after post layout simulation. The step used for creating designs are: schematic, layout, design rule check (DRC), layout vs schematic (LVS) and QRC for parasitic extracted view of layout. RSNM and HSNM of 10T SRAM cell are 0.42V. RSNM of 10T SRAM cell is found maximum among all SRAM cells. Average write delay is the average of write 1 delay and write 0 delay. Write 1 delay is the time require for changing data at the internal node of SRAM cell from low value to high value. Similarly, the write 0 delay is time require for changing the data at internal node from high value to low value. Write delay is measured between

TABLE I. COMPARISON OF PARAMETERS FOR DIFFERENT SRAM CELL

Parameters	6T	7T	8T	9T	10T
RSNM (V)	0.21	0.07	0.41	0.41	0.42
HSNM (V)	0.41	0.42	0.41	0.41	0.42
Write 1 delay (ps)	87.69	124.26	93.63	93.15	94.06
Write 0 delay (ps)	57.85	77.33	61.97	60.39	55.82
Avg. Write delay (ps)	72.77	100.79	77.80	76.77	74.94
Rise time (ps)	51.89	103.08	67.27	60.90	61.15
Fall time (ps)	51.89	103.08	67.27	60.90	61.15
Avg. Dynamic Power (W)	113.77n	194.68n	9.06μ	0.85μ	154.31n
Static Power (μW)	1.51	1.14	1.26	1.14	1.14
Total Power Dissipation (μW)	1.63	1.33	10.33	11.99	1.29
Width (μm)	3.27	3.8	2.55	2.35	3.37
Height (μm)	3.04	3.83	3.17	3.92	3.06
Surface Area (μm^2)	9.93	14.54	8.07	9.18	10.30
Supply Voltage (V)	1	1	1	1	1
Technology	45nm	45nm	45nm	45nm	45nm

word line WL and internal node P of SRAM cell. The rise time and fall time for 6T SRAM cell are found minimum, at 51.89 ps. But 7T SRAM cell has maximum average write as well as fall and rise time. Total power dissipation of 10T SRAM cell is 1.29 μW which is least among all memory cells. To minimize the surface area of SRAM cell finger method is used which also reduces the parasitic capacitance of the circuit. Layout area of cells is calculated in width (μm), height (μm) and surface area (μm^2). After the comparison it is found that surface area of 7T SRAM cell is maximum, which is 14.54 μm^2. Fig.27 shows the graphical comparison of SNM during read, hold operation and total power dissipation for different SRAM cells. This illustrates that the RSNM of 7T cell is lowest compared to other memory cells. RSNM of 8T, 9T and 10T have nearly same level. 9T SRAM cell has largest total power dissipation 11.99 μW . Power dissipation is greatest for 9T cell and lowest for 10T cell.

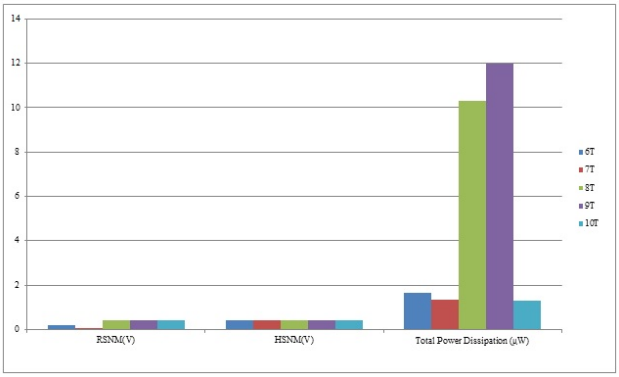

Figure 27. Graphical comparison for RSNM, HSNM and total power dissipation of different SRAM Cell

Fig.28 illustrates the graphical comparison for layout of different SRAM cell in their respective weight, height and surface area. Surface area of 7T SRAM cell has highest peak and 8T has minimum peak. The finger method is used to reduce the size of transistor, in this method transistors are arranged such as one terminal is common between two transistors which acts as source for one transistor and drain for the other. Due to sharing of terminal, parasitic capacitance of source to body and drain to body reduces to half of its value. Layout area of 10T cell is only less than 7T cell but it has good write delay, rise and fall time, it has also maximum RSNM and minimum total power dissipation.

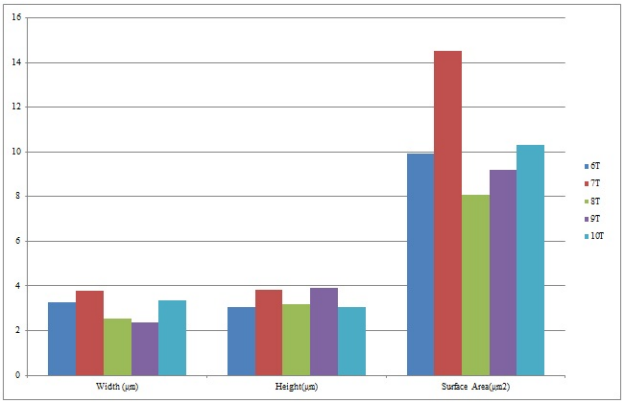

Figure 28. Graphical comparison of layout for different SRAM Cell

After the comparison, it is noticed that 10T cell has better RSNM, average write delay, power dissipation when compared to other SRAM cell at the price of slightly rise in surface area. 10T cell has large surface area in comparison with 6T, 7T and 8T cells. Layout of 4×4 array using 6T cell has surface area of 295.75 μm^2. Layout of SRAM using 4×4 array of 6T SRAM cell has surface area of 606.84 μm^2. Comparison for 6T, 8T and 9T SRAM cell is done with [16]. RSNM and Write delay are compared as shown in table II.

TABLE II. COMPARISON OF PARAMETERS OF DIFFERENT SRAM CELL

Parameters	6T	6T[16]	8T	8T[16]	9T	9T[16]
Technology	45nm	90nm	45nm	90nm	45nm	90 nm
RSNM(V)	0.18	0.037	0.37	0.228	0.36	0.217
Write Delay(ps)	72.77	8.976	77.80	45.47	76.77	10

It is found that RSNM for 6T, 8T, 9T SRAM is much better in this work but there is an increase in write delay for 6T, 8T, 9T SRAM in this work. The RSNM value in table II is taken after process corner simulations as shown in Fig.31, 33, 34 for 6T, 8T and 9T SRAM cell.

Graphical comparison for RSNM and write delay for 6T, 8T and 9T with [16] in table II is represented in fig.29 and fig.30.

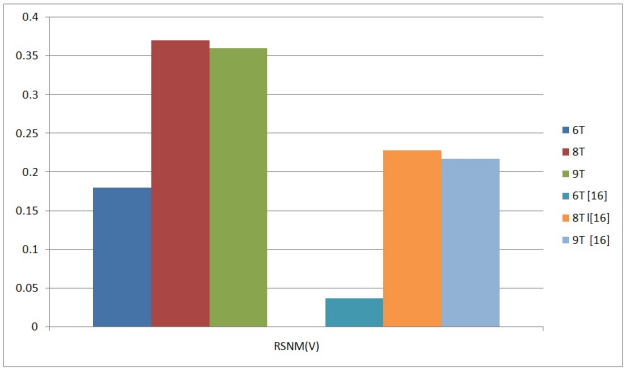

Figure 29. Graphical comparison of RSNM for different SRAM Cell with [16]

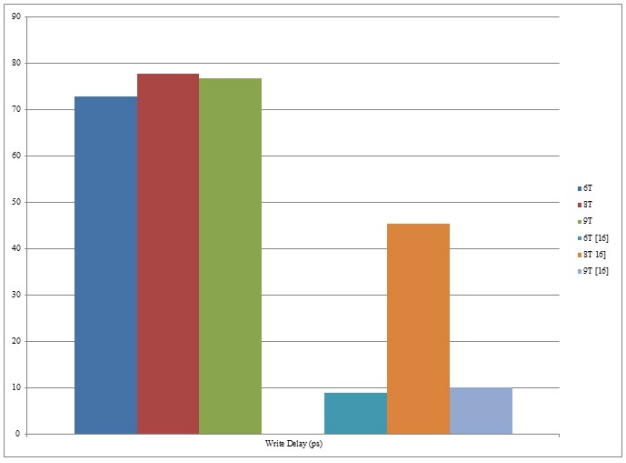

Figure 30. Graphical comparison of write delay for different SRAM Cell with [16]

CNFET based 10T SRAM has total power dissipation is 22.48nW, in which, the static power is 0.46nW and average dynamic power is 22.02nW. For CNTFET 11nm technology is used with 0.3V voltage supply. This power dissipation is less compared to MOSFET based SRAM cell. Write 0 delay is 519.1ps, Write 1 delay is 171.1ps and average write delay is 345.1ps. Rise time is 529.1ps and fall time is 197.9ps. The write delay, rise time and fall time are greater as compared to the MOSFET based SRAM cells.

A. Process variation

The process corner analysis shows whether the circuit is tolerant to fabrication process corner variation. Process variation is done for checking the performance of the circuit in different corners, these are: monte corlo (MC), slow slow (SS), slow fast (SF), fast slow (FS), and fast fast (FF). Process variation is done for 6T, 7T, 8T, 9T and 10T cells. In process variation of different corner simulations of these cells are performed for RSNM analysis. RSNM value is calculated from the side of the square inside the butterfly curve. There are two squares formed in the butterfly curve, square which has less sides is taken for the RSNM value. Fig.31 illustrates the corner simulation waveform of 6T cell is read mode. It is fournd that 6T design has 0.18V of RSNM between FF and FS corner simulation.

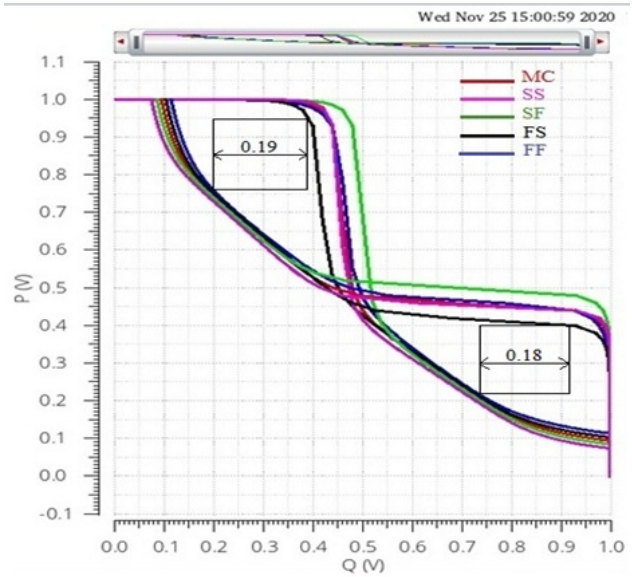

Figure 31. Corner simulation of 6T Cell in read mode

Square window of butterfly in 7T SRAM cell for corner simulation in read process is shown in fig.32. It is formed between SF and FS corner simulation. Minimum square

formed, which has 0.01 V of RSNM available to read the data. In the process variation it is found that 7T SRAM cell has very less RSNM.

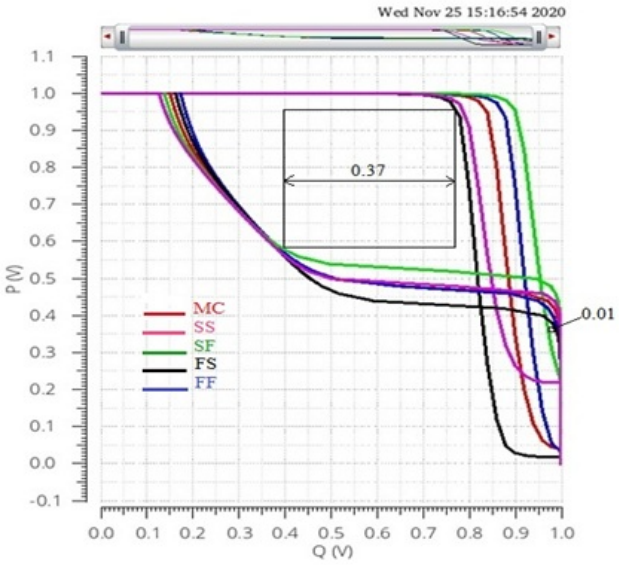

Figure 32. Corner simulation of 7T SRAM Cell in read mode

Fig.33 shows the corner simulation of 8T SRAM cell. Square of 0.37V RSNM is formed between SF and FS. This is better RSNM than 6T and 7T SRAM cell. This value is sufficient to perform read operation. Data is stable during read operation.

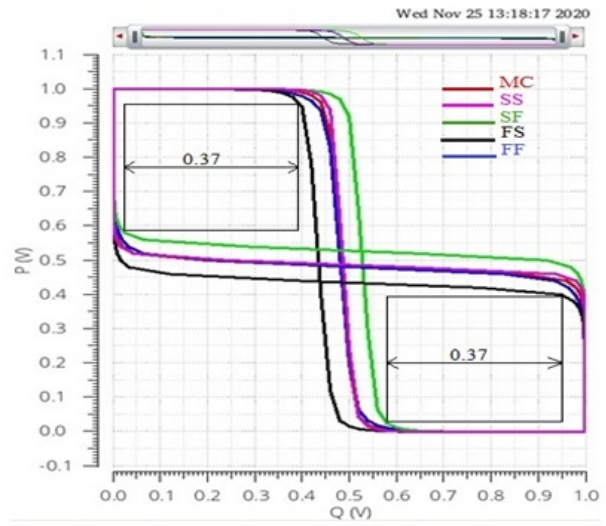

Figure 33. Corner simulation waveform of 8T SRAM Cell in read mode

Fig.34 represents the corner simulation waveform of 9T cell. Minimum size of square formed in butterfly is 0.36V. It is a good value for read operation. There is no data retention problem. This square is formed between SF and FS corner simulation during read process. Data is stable during read operation.

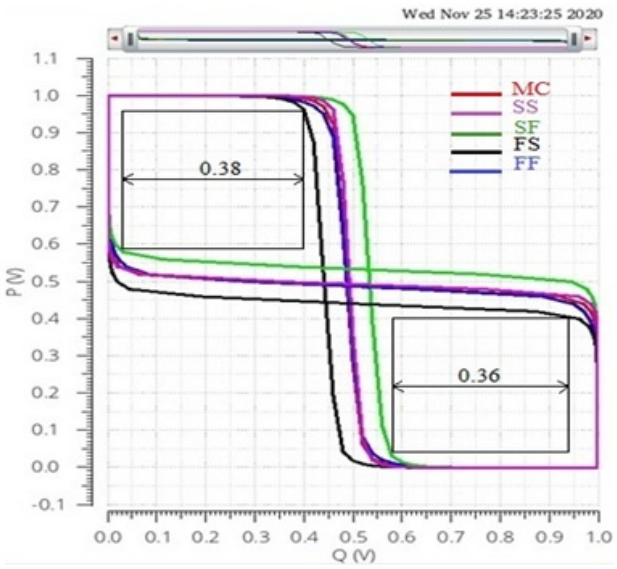

Figure 34. Corner simulation waveform of 9T SRAM Cell in read mode

Fig.35 shows the corner simulation of 10T SRAM cell. Minimum size of square formed in butterfly is 0.37V. It is good value for read the data from SRAM cell. 10T SRAM has 0.37 V of RSNM formed between SF and FS corner simulation during read operation. Data is stable during read operation.

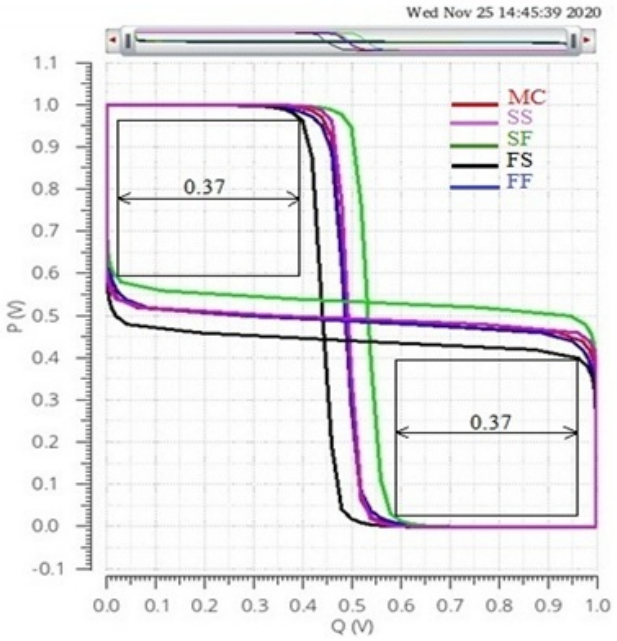

Figure 35. Corner simulation of 10T SRAM Cell in read mode

B. Monte Carlo analysis

Monte Carlo analysis is a statistical way to examine any design. This simulation is done for testing the circuit in process variation and check the robustness of the device. Monte Carlo analysis and simulation of 6T, 7T, 8T, 9T and 10T cell are carried out for these parameters- average dynamic power, static power, rise time and fall time. This analysis is carried out for 2000 samples with sigma (σ) equal to 3. This simulation shows the value of mean and standard deviation. Deviation of the samples should not very far from the mean. Most of the samples should lie inside three sigma (3σ) range. This simulation shows the normal distribution curve and histogram representation of the samples with in 3σ range. This gives a clear idea of the samples where they are lying during the simulation. All the results based on this simulation are shown in the table III. Fig.36, 37, 38, 39 represents the simulation of Monte Carlo for 6T cell for its parameters.

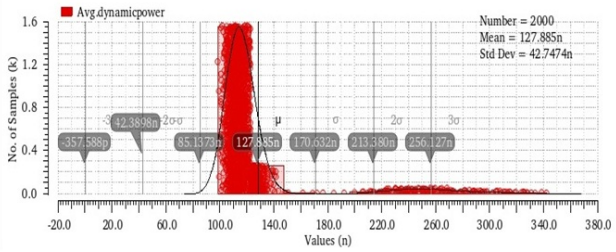

Figure 36. Monte Carlo of 6T Cell for average dynamic power

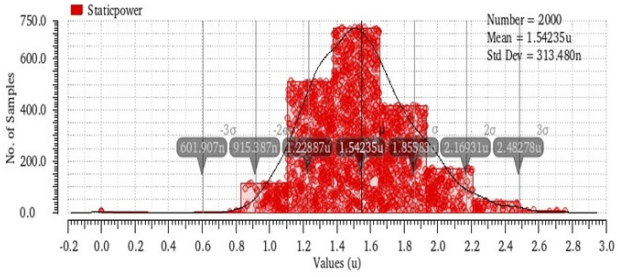

Figure 37. Monte Carlo of 6T Cell for static power

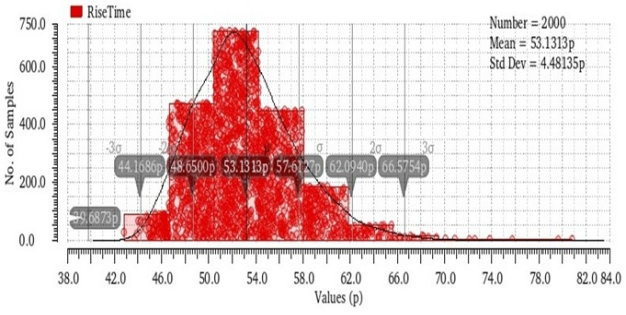

Figure 38. Monte Carlo of 6T Cell for rise time

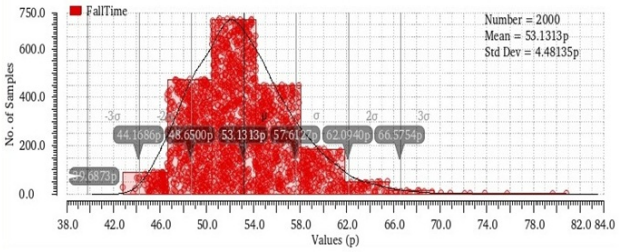

Figure 39. Monte Carlo of 6T Cell for fall time

Fig.40, 41, 42, 43 represents the simulation of Monte Carlo for 7T memory cell for its parameters.

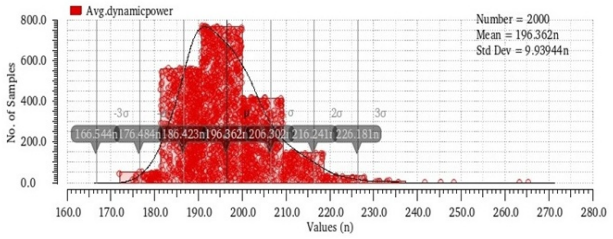

Figure 40. Monte Carlo of 7T Cell for average dynamic power

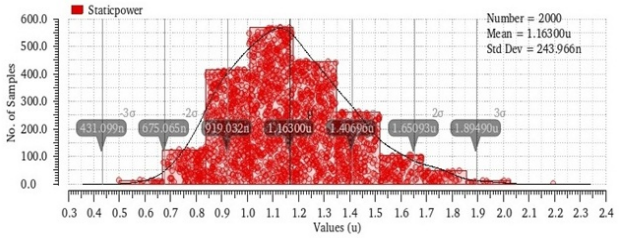

Figure 41. Monte Carlo of 7T Cell for static power

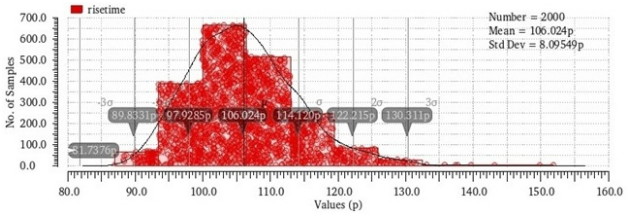

Figure 42. Monte Carlo of 7T Cell for rise time

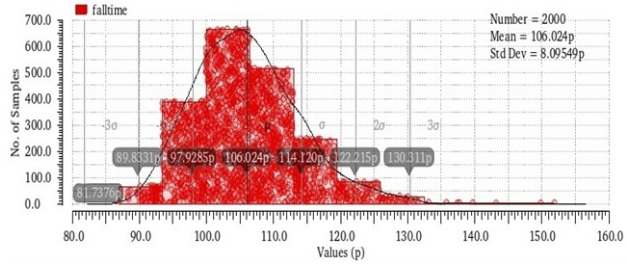

Figure 43. Monte Carlo of 7T Cell for fall time

Fig.44, 45, 46, 47 represents the simulation of Monte Carlo for 8T memory cell for its parameters.

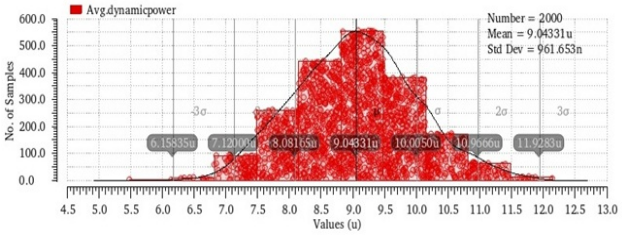

Figure 44. Monte Carlo of 8T Cell for average dynamic power

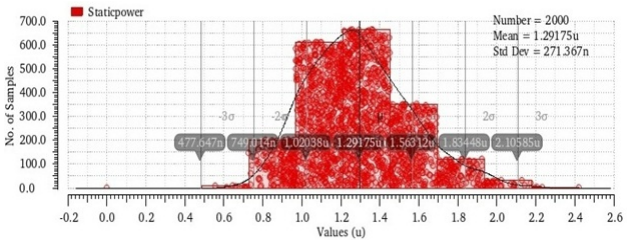

Figure 45. Monte Carlo of 8T Cell for static power

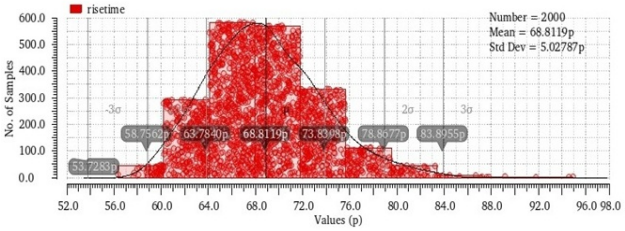

Figure 46. Monte Carlo of 8T SRAM Cell for rise time

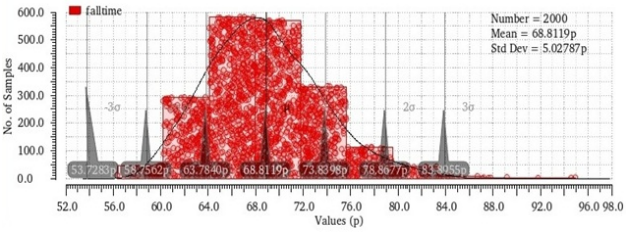

Figure 47. Monte Carlo of 8T Cell for fall time

Fig.48, 49, 50, 51 represents the simulation of Monte Carlo for 9T memory cell for its parameters.

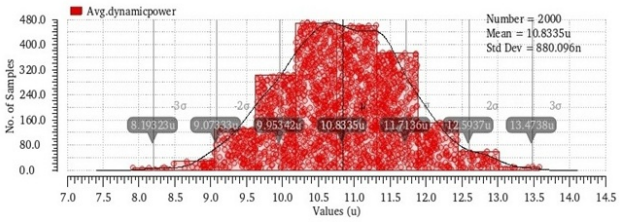

Figure 48. Monte Carlo of 9T Cell for average dynamic power

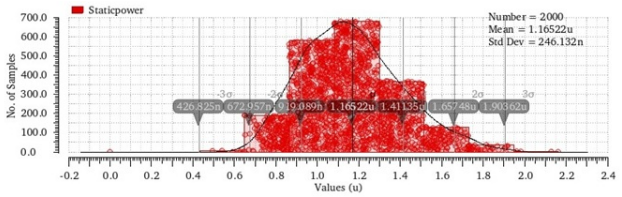

Figure 49. Monte Carlo of 9T Cell for static power

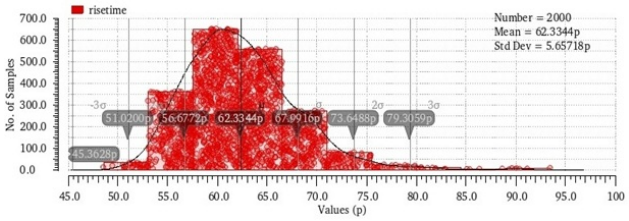

Figure 50. Monte Carlo of 9T Cell for rise time

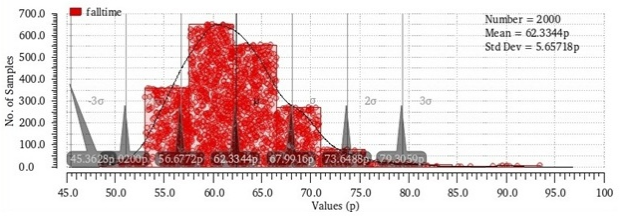

Figure 51. Monte carlo of 9T Cell for fall time

Fig.52, 53, 54, 55 represents the simulation of Monte Carlo for 10T memory cell for its parameters.

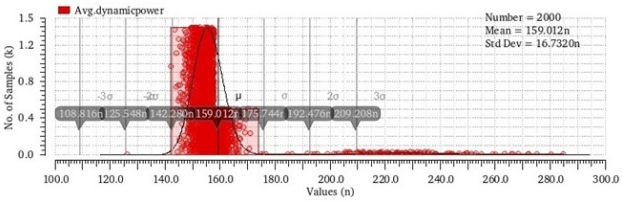

Figure 52. Monte Carlo of 10T Cell for average dynamic power

TABLE III. MONTE CARLO ANALYSIS WITH 2000 SAMPLES FOR DIFFERENT SRAM CELL

Parameters	6T		7T		8T		9T		10T	
	(M)	(σ)	(M)	(σ)	(M)	(σ)	(M)	(σ)	(M)	(σ)
Avg.Dynamic Power(W)	127.89n	42.75n	196.36n	9.94n	9.04μ	961.65n	10.83μ	880.10n	159.01n	16.73n
Static Power(W)	1.54μ	313.48n	1.16μ	243.97n	1.29μ	271.37n	1.17μ	246.13n	1.17μ	243.41n
Rise Time(ps)	53.13	4.48	106.02	8.10	68.81	5.028	62.33	5.66	62.61	6.02
Fall Time(ps)	53.13	4.48	106.02	8.10	68.81	5.028	62.33	5.66	62.61	6.02

TABLE IV. PARAMETERS DEVIATION FROM MEAN IN MONTE CARLO SIMULATIONS

Parameters	6T	7T	8T	9T	10T
	M-3σ	M-3σ	M-3σ	M-3σ	M-3σ
Avg. Dynamic Power(nW)	-0.36	166.54	6155.05	8189.7	108.82
Static Power(μW)	0.60	0.43	0.48	0.43	0.44
Rise Time(ps)	39.69	81.72	53.726	45.35	44.55
Fall Time(ps)	39.69	81.72	53.726	45.35	44.55

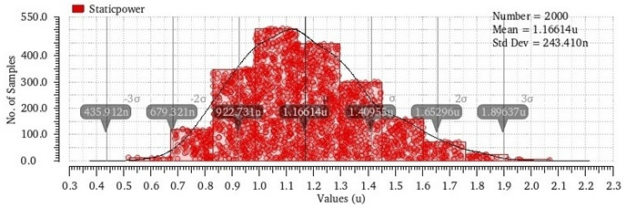

Figure 53. Monte Carlo of 10T Cell for static power

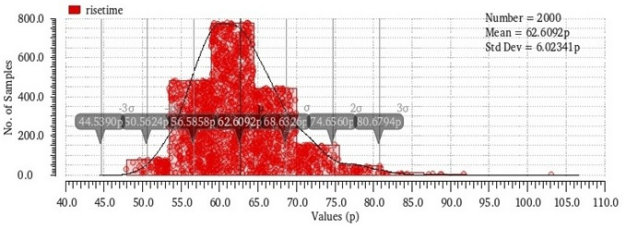

Figure 54. Monte Carlo of 10T Cell for rise time

Table III shows the Monte Carlo analysis for 6T, 7T, 8T, 9T and 10T cells with respect to average dynamic power, static power, rise time and fall time. This simulation is carried out using 2000 samples for SRAM cells using three sigma method. It gives the value of mean(M) and standard deviation(σ) with respect to their parameter. Table IV shows the standard deviation from the mean for SRAM cells. Here M-3(σ) value is calculated for SRAM cells. There is a negative sign in 6T SRAM cell during Monte Carlo analysis for average dynamic power. It shows that the deviation in average dynamic power from its mean is more. Remaining all simulation for all SRAM cells have positive sign. It shows that there is deviation in parameters which are not very far from its mean value.

So, after analysis of all the parameters, it is observed that 10T SRAM design has best performance. It has low total power of dissipation because of its low static and dynamic powers. This design has positive difference between mean and standard deviation for all the parameters; it has less standard deviation from its mean value.

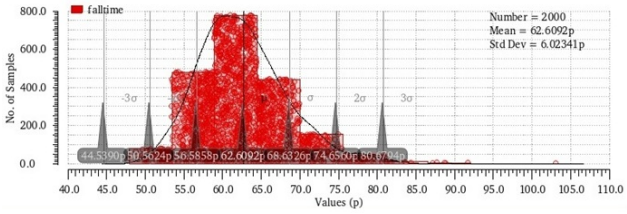

Figure 55. Monte Carlo of 10T Cell for fall time

6. CONCLUSION

In this paper 6T, 7T, 8T, 9T and 10T cells of SRAM are implemented using CMOS 45nm Technology. Finger method is used to create the layout of these SRAM cells. This method helps in decreasing the surface area of the device and reducing the parasitic in layout design. After the comparison of parameters in respect of their RSNM, HSNM, average write delay, total power dissipation, width, height and surface area, rise time and fall time, it is inspected that 10T cell has 1.29μW total power dissipation which is least among SRAM cells. It has 0.42V of static noise margin for both read and hold process. There is a symmetry in both the square of butterfly curve during read and hold mode. The data retention during read operation in 10T cell is found maximum as compare to other SRAM cells. Average write delay of 10T SRAM cell is 74.94ns which is also comparatively better than other SRAM cells except 6T cell. 6T cell has 72.77ns of average write delay which is little less than 10T Cell. 7T cell has minimum 0.07V of RSNM which is very less to retain data in read mode. For clear view of RSNM, corner simulation is performed. From the simulation of different process variations, it is clear that 10T SRAM cell is best among other cells and 7T SRAM cell is the worst RSNM. Monte Carlo simulation is carried out using 2000 samples to find the deviation in parameters with their mean value. In

this simulation, 10T SRAM cell has better performance. Parameters used in Monte Carlo simulations are average dynamic power, static power, rise time and fall time. 8T SRAM cell has less surface area which is $8.07\mu m^2$ but it has total power dissipation greater than 10T SRAM cell. SRAM is implemented using 4×4 array of 6T SRAM cell which has a surface area of $606.84\mu m^2$. 6T, 8T and 9T SRAM cells are compared with [16] in respect to their RSNM and write delay. RSNM in this work is better than [16] with the price of write delay. CNTFET based 10T SRAM cell is simulated which has less power dissipation which is 22.48nW at 0.3V of supply voltage.

References

[1] K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake, "A read-static-noise-margin-free sram cell for low-vdd and high-speed applications," *IEEE journal of solid-state circuits*, vol. 41, no. 1, pp. 113–121, 2005.

[2] S. Pal and A. Islam, "Variation tolerant differential 8t sram cell for ultralow power applications," *IEEE transactions on computer-aided design of integrated circuits and systems*, vol. 35, no. 4, pp. 549–558, 2015.

[3] S. Strangio, P. Palestri, D. Esseni, L. Selmi, F. Crupi, S. Richter, Q.-T. Zhao, and S. Mantl, "Impact of tfet unidirectionality and ambipolarity on the performance of 6t sram cells," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 223–232, 2015.

[4] S. Pal and A. Islam, "9-t sram cell for reliable ultralow-power applications and solving multibit soft-error issue," *IEEE Transactions on Device and Materials Reliability*, vol. 16, no. 2, pp. 172–182, 2016.

[5] C. Kushwah and S. K. Vishvakarma, "A single-ended with dynamic feedback control 8t subthreshold sram cell," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 1, pp. 373–377, 2015.

[6] T. W. Oh, H. Jeong, J. Park, and S.-O. Jung, "Pre-charged local bit-line sharing sram architecture for near-threshold operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 10, pp. 2737–2747, 2017.

[7] G. Pasandi, R. Mehta, M. Pedram, and S. Nazarian, "Hybrid cell assignment and sizing for power, area, delay-product optimization of sram arrays," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 12, pp. 2047–2051, 2019.

[8] Y. Yang, J. Park, S. C. Song, J. Wang, G. Yeap, and S.-O. Jung, "Single-ended 9t sram cell for near-threshold voltage operation with enhanced read performance in 22-nm finfet technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 11, pp. 2748–2752, 2014.

[9] A. Singh, M. K. Jain, and S. Wairya, "Novel lossless grounded and floating inductance simulators employing a grounded capacitor based on cc-cfa," *Journal of Circuits, Systems and Computers*, vol. 28, no. 06, p. 1950093, 2019.

[10] N. K. Misra, B. Sen, and S. Wairya, "Novel conservative reversible error control circuits based on molecular qca," *International Journal of Computer Applications in Technology*, vol. 56, no. 1, pp. 1–17, 2017.

[11] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mv robust schmitt trigger based subthreshold sram," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, 2007.

[12] S. Lin, Y.-B. Kim, and F. Lombardi, "A 32nm sram design for low power and high stability," in *2008 51st Midwest Symposium on Circuits and Systems*. IEEE, 2008, pp. 422–425.

[13] A. Agarwal and K. Roy, "A noise tolerant cache design to reduce gate and sub-threshold leakage in the nanometer regime," in *Proceedings of the 2003 International Symposium on Low Power Electronics and Design, 2003. ISLPED'03.* IEEE, 2003, pp. 18–21.

[14] K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepalli, Y. Wang, B. Zheng, and M. Bohr, "Sram design on 65-nm cmos technology with dynamic sleep transistor for leakage reduction," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 895–901, 2005.

[15] E. Morifuji, D. Patil, M. Horowitz, and Y. Nishi, "Power optimization for sram and its scaling," *IEEE Transactions on Electron Devices*, vol. 54, no. 4, pp. 715–722, 2007.

[16] P. Athe and S. Dasgupta, "A comparative study of 6t, 8t and 9t decanano sram cell," in *2009 IEEE Symposium on Industrial Electronics & Applications*, vol. 2. IEEE, 2009, pp. 889–894.

[17] Z. Liu and V. Kursun, "Characterization of a novel nine-transistor sram cell," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 16, no. 4, pp. 488–492, 2008.

[18] R. Giterman, M. Vicentowski, I. Levi, Y. Weizman, O. Keren, and A. Fish, "Leakage power attack-resilient symmetrical 8t sram cell," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2180–2184, 2018.

[19] F. Frustaci, M. Khayatzadeh, D. Blaauw, D. Sylvester, and M. Alioto, "Sram for error-tolerant applications with dynamic energy-quality management in 28 nm cmos," *IEEE Journal of Solid-state circuits*, vol. 50, no. 5, pp. 1310–1323, 2015.

[20] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read stability and write-ability analysis of sram cells for nanometer technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, 2006.

[21] W.-X. You, P. Su, and C. Hu, "A new 8t hybrid nonvolatile sram with ferroelectric fet," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 171–175, 2020.

[22] A. Rajendran, Y. Shiyanovskii, F. Wolff, and C. Papachristou, "Noise margin, critical charge and power-delay tradeoffs for sram design," in *2011 IEEE 17th International On-Line Testing Symposium*. IEEE, 2011, pp. 145–150.

[23] S.-M. Kang and Y. Leblebici, *CMOS digital integrated circuits*. Tata McGraw-Hill Education, 2003.

[24] S. S. Sakhare, K. Miyaguchi, P. Raghavan, and A. Mercha, "Simplistic simulation-based device-vt-targeting technique to determine technology high-density lele-gate-patterned finfet sram in sub-10 nm era," *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1716–1724, 2014.

[25] M. Kumar and J. S. Ubhi, "Performance evaluation of 6t, 7t & 8t sram at 180 nm technology," in *2017 8th International Conference*

on Computing, Communication and Networking Technologies (ICCCNT). IEEE, 2017, pp. 1–6.

[26] L. Wei, D. J. Frank, L. Chang, and H.-S. P. Wong, "A non-iterative compact model for carbon nanotube fets incorporating source exhaustion effects," in *2009 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2009, pp. 1–4.

[27] G. Hills, M. G. Bardon, G. Doornbos, D. Yakimets, P. Schuddinck, R. Baert, D. Jang, L. Mattii, S. M. Y. Sherazi, D. Rodopoulos *et al.*, "Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital vlsi," *IEEE Transactions on Nanotechnology*, vol. 17, no. 6, pp. 1259–1269, 2018.

[28] C. Lau, T. Srimani, M. D. Bishop, G. Hills, and M. M. Shulaker, "Tunable n-type doping of carbon nanotubes through engineered atomic layer deposition hfox films," *ACS nano*, vol. 12, no. 11, pp. 10 924–10 931, 2018.

[29] H. Wei, M. Shulaker, H.-S. P. Wong, and S. Mitra, "Monolithic three-dimensional integration of carbon nanotube fet complementary logic circuits," in *2013 IEEE International Electron Devices Meeting*. IEEE, 2013, pp. 19–7.

[30] A. G. Amer, R. Ho, G. Hills, A. P. Chandrakasan, and M. M. Shulaker, "29.8 sharc: Self-healing analog with rram and cnfets," in *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE, 2019, pp. 470–472.

[31] B. H. Calhoun and A. P. Chandrakasan, "Static noise margin variation for sub-threshold sram in 65-nm cmos," *IEEE Journal of solid-state circuits*, vol. 41, no. 7, pp. 1673–1679, 2006.

[32] G. V. Luong, S. Strangio, A. Tiedemann, P. Bernardy, S. Trellenkamp, P. Palestri, S. Mantl, and Q. Zhao, "Strained silicon complementary tfet sram: Experimental demonstration and simulations," *IEEE journal of the Electron Devices Society*, vol. 6, pp. 1033–1040, 2018.

[33] A. Grover, G. Visweswaran, C. R. Parthasarathy, M. Daud, D. Turgis, B. Giraud, J.-P. Noel, I. Miro-Panades, G. Moritz, E. Beigné *et al.*, "A 32 kb 0.35–1.2 v, 50 mhz–2.5 ghz bit-interleaved sram with 8 t sram cell and data dependent write assist in 28-nm utbb-fdsoi cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2438–2447, 2017.

[34] Z. Ghaderi, N. Bagherzadeh, and A. Albaqsami, "Stable: Stress-aware boolean matching to mitigate bti-induced snm reduction in sram-based fpgas," *IEEE Transactions on Computers*, vol. 67, no. 1, pp. 102–114, 2017.

[35] D. Takashima, M. Endo, K. Shimazaki, M. Sai, and M. Tanino, "A 7t-sram with data-write technique by capacitive coupling," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 596–605, 2018.

[36] H. Mori, T. Nakagawa, Y. Kitahara, Y. Kawamoto, K. Takagi, S. Yoshimoto, S. Izumi, H. Kawaguchi, and M. Yoshimoto, "A 28-nm fd-soi 8t dual-port sram for low-energy image processor with selective sourceline drive scheme," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 4, pp. 1442–1453, 2018.

[37] C.-H. Yu, P. Su, and C.-T. Chuang, "Impact of random variations on cell stability and write-ability of low-voltage srams using monolayer and bilayer transition metal dichalcogenide (tmd) mosfets," *IEEE Electron Device Letters*, vol. 37, no. 7, pp. 928–931, 2016.

[38] Y. Sun, H. Jiao, and V. Kursun, "A novel robust and low-leakage sram cell with nine carbon nanotube transistors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 9, pp. 1729–1739, 2014.

[39] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold sram design for ultra-low-voltage operation," *IEEE journal of solid-state circuits*, vol. 42, no. 3, pp. 680–688, 2007.

[40] P. S. Kanhaiya, C. Lau, G. Hills, M. D. Bishop, and M. M. Shulaker, "Carbon nanotube-based cmos sram: 1 kbit 6t sram arrays and 10t sram cells," *IEEE Transactions on Electron Devices*, vol. 66, no. 12, pp. 5375–5380, 2019.

Anurag Yadav Anurag Yadav received his B.Tech degree in Electronics and Communication Engineering from the Uttar Pradesh Technical University, Lucknow, India in 2008. He received his Master of Engineering degree in Electronics and Communication Engineering from Panjab University, (National Institute of Technical Teachers Training and Research, Chandigarh), Chandigarh, India. He is currently pursuing Ph.D. in field of Electronics Engineering from Institute of Engineering and Technology, Dr. A.P.J. Abdul Kalam Technical University, Lucknow, India. His current research interests include VLSI Design, Digital IC design and Analog IC design.

Dr. Subodh Wairya Dr. Subodh Wairya received his B.Tech in Electronics Engineering from HBTI, Kanpur in 1993. He had received his M.E. (Tele-Communication Engineering) from Jadavpur University, Kolkata. He had also received his Ph.D. in field of Electronics Engineering from Motilal Nehru National Institute of Technology, Allahabad and currently serving as Professor in Institute of Engineering and Technology, Lucknow. His current research interests include VLSI Design, High Speed Network and Image Processing.