



An Innovative Design of Low Power Binary Adder based on Switching Activity

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Abstract: A binary adder is a primary component of many high-performance architectures like Digital Signal Processing (DSP), Image Processing, and Multimedia Processing. The design of a suitable binary adder in terms of power dissipation, delay, energy efficiency, and silicon chip area is more challenging. To obtain better performance metrics, a new full adder circuit design has been introduced in this paper. Here, three full adder designs are developed based on the Switching Activity (SA) of basic logic gates (AND, OR, and NOT). The SA value of the NOT gate is large compared to the other two logic gates. The proposed full adder is developed based on the logic decomposition method, which reduces the number of NOT gates as well as the overall SA value in the binary adder circuit, which leads to a reduction in dynamic power dissipation and the area of the binary adder circuit. In this paper, three 1-bit Full Adders are designed and their behaviour is described using Verilog HDL, synthesised and implemented in a Xilinx Vivado Zynq-7000 family configurable device. The implementation results indicate that the proposed full adder design yields better performance in comparison with Conventional Full Adder (CFA) and Modified Conventional Full Adder (MCFA) in terms of cell count, delay, power dissipation, and Energy Delay Product (EDP). The proposed full adder is attractive in improving 58.8% in Standard Basic Cell Count (SBCC), 65.9% in dynamic power dissipation and 66% in PDP compared to conventional method and 22.2% in SBCC, 43.8% in dynamic power dissipation and 43.9% in PDP compared to the modified conventional method. Furthermore, a formula-based evaluation is made on performance metrics to get optimal design trade-offs in terms of EDP. The EDP of the proposed full adder is reduced by 66.1% compared to the conventional method and by 44% compared to the modified conventional method.

Keywords: Dynamic Power, EDP, Full Adder, SA, SBCC

1. INTRODUCTION

The primary goal of digital designers is to develop optimizing digital circuits and model them as energy efficient, smaller and faster. Figure 1 shows a typical area, delay and power as logical metrics after hardware synthesis. In figure 1 the optimal design tradeoff points are defined by using 3-D Co-Ordinates. The execution of digital systems can be improved by the proper draft of logic design. Generally, the critical concerns of Very Large Scale Integration (VLSI) circuit design engineers are minimized circuit area, intensification of performance, and reliability upgrading.

The eruptive growth in portable devices like personal gadgets has raised the research endeavour in low power micro devices. With the combustible advancement of device scaling, the research work of microelectronic circuit designs has been elaborately mounted. A binary Full Adder (FA) is enormously used element of binary addition, since it is a basic cell for building large bit size adders and multipliers [1][2]. Hence, performance intensification of FA is critical to the performance of refinement of the Central Processing

Unit (CPU) and DSP architectures in microprocessors. The standard design of FA is usually numerous [3]. In the rapid growth and manifold applications of VLSI computational circuits and processors, the adder plays a crucial role. The primary goal of the adder is to perform the addition of two binary numbers. It is also used in multiple operations such as address calculation of cache or memory access units, multiplication, subtraction, and division [4]. Hence, there is a need to design a fast and minimum power dissipated full adder circuit. The Basic Cell Count (BCC), which is one of the feature aspects, governs the system difficulty of arithmetic circuits like multipliers and ALU. Power dissipation and delay would be another two dominant factors when it comes to advances in the design of arithmetic circuits, although they have a contrasting relationship with one another. Consequently, Energy Delay Product (EDP) and Power Delay Product (PDP) have been used to obtain optimal design performance metrics. The rest of the paper is arranged as follows: Section 2 addresses the motivation and literature review of the work. Some of the important preliminaries are discussed in section 3.

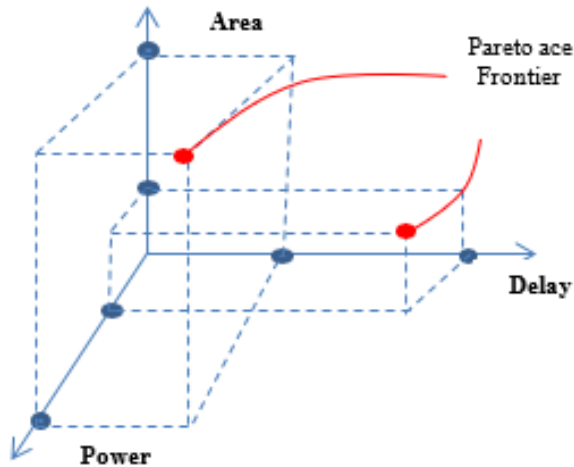


Figure 1. The delineate tradeoff points between Area, Delay and Power

The detailed explanations of three full adder designs are reported in section 4. In section 5, the simulation results and theoretical analysis are discussed.

2. STATE OF BACKGROUND WORK

In this section, the theme of the paper and literature review are discussed.

A. Motivation of the work

The execution of digital logic circuits can be improved by the proper draft of logic design style. The logic design styles are assorted in the practice of computing in-between cells, the cell count, but they are executing the same functionality. It is comprehensible to see the Switching Activity (SA) of the NOT cell and its value is 0.25. It is desirable to reduce the use of NOT cell count in logic circuits during the design process, as it eventually leads to minimize the SA of the whole digital circuit as well as cell count. This concept is clearly explained in the following sections with an example.

B. Literature Review

Evaluation of designs in terms of cell count and power dissipation at multiple levels of abstraction and system unification is presented in [5]. Combinatorial circuit designs have vigor and diversify. It gives enlightenment and the conduct for other circuit designs, discussed in [6]. Quick-witted rule based algorithm for minimizing SA of digital logic circuits at logic style optimization, reported in [7]. An efficient carry save multiplier with area, critical path delay, and power-energy efficient architectures using modified Conventional Full Adder (CFA) and improved FA is presented in [8]. Reduction of power dissipation in CMOS digital logic circuits, deliberated in the past, by examining the logic level, circuit level, and physical level of designs [9][10]. An evaluation of different practises in low power CMOS circuit design is also described in [11]. In digital logic circuits, minimization of the mean of switching

transitions of VLSI circuit nodes is reported in [12]. An evaluation of the mean SA in memory-less and memory-sequential circuits under arbitrary input orders is conferred in [13] using the extensive delay model. A systematic approach to the estimation of glitches and the relation between them is introduced in [14]. The design method in [15] furnishes an interesting archive of contemporary techniques of power abstraction and low power motif based on synthesis. The assessment and the switching from 0 ! 1 and 1 ! 0 at any junction is suggested in [16]. In order to assure the classical probabilistic perspective that restricts the utmost value of SA to one meaning, as presented in [16] was tailored in [17]. An algorithmic perspective at the logic gate level simplification using Karnaugh maps for minimizing the SA in a combinatorial logic circuit is proposed in [18] and about ten percent reduction in SA at logic gate level is also described in [19]. In [20] a method to compute the SA using an irregular delay model is described.

3. PRELIMINARIES

The power and energy consumption of digital logic circuits and the concept of switching activity are explained in the following section.

A. Power and Energy consumption

The total Power dissipation (P) of digital VLSI circuits consists of two basic components: static [8] and dynamic [17]. Hence,

$$P = P_s + P_d \quad (1)$$

Where, P_s Denote static power consumption, P_d Stands dynamic power consumption.

Energy consumption (E_c) of a digital VLSI circuit can be defined as

$$E_c = P \quad t = P \quad \frac{1}{f} \quad (2)$$

Where, f represents frequency and t denotes period.

Static Component

Static energy dissipation appears as a direct consequence of leakage currents (I_{leak}) during the steady state of a Metal Oxide Semiconductor (MOS) transistor. Leakage current takes place when there is no switching in the input state. It is seeded by several components of the CMOS transistor and is given by

$$I_{leak} = I_R + I_{sub} + I_G + I_{gidl} \quad (3)$$

Where, I_R is leakage current due to reverse bias diodes, I_{sub} indicates the current due to sub threshold condition, I_G represents a Gate leakage current, I_{gidl} denotes the leakage current due to gate induced drain lowering.

Static power dissipation (P_s) Of MOS transistor drawn from the supply voltage (V_{dd}) is expressed as

$$P_s = I_{leak} \quad V_{dd} \quad (4)$$

Static energy (E_s) dissipation can be calculated as

$$E_s = P_s \cdot T = I_{leak} \cdot V_{dd} \cdot T \quad (5)$$

Where, T denotes the duration of time

Dynamic Component

Based on input signals, logic 1 is generated by charging the C_L through Pull Up Network (PUN) and logic 0 is generated by discharging C_L Through Pull Down Network (PDN). During the charging process, energy is pinched from the supply voltage V_{dd} , which is $V_{dd}^2 \cdot C_L$.

In duration of time T , dynamic power dissipation [3][4] is obtained as follows

$$P_d = \frac{1}{T} \int_0^T v(t) \cdot i(t) \cdot dt = \frac{V_{dd}^2 \cdot C_L}{T} \quad (6)$$

In duration of time T , if the output node switch n times, then the amount of power pinched from the supply voltage is $n \cdot V_{dd}^2 \cdot C_L$.

Consequently, the amount of dynamic power dissipated during the charging and discharging process from number of times is represented as:

$$P_d = n \cdot V_{dd}^2 \cdot C_L \cdot f \quad (7)$$

Let us assume that the chip works at the frequency of the clock signal and in time T , the number of transitions (k) by the clock signal is given by

$$k = f \cdot T_{clk} \quad (8)$$

Using (8) in (7) gives

$$P_d = V_{dd}^2 \cdot C_L \cdot f_{clk} \quad (9)$$

Where

$$= \frac{n}{k}$$

indicates the switching activity factor

In the current day technology 80% of power dissipation [9] [10] [16] happens due to switching activity [13]. In order to minimize the power loss of CMOS circuits, it is prudent to reduce the SA factor of VLSI circuits.

B. Switching Activity

It is defined based on the probability of logic occurrence of a '0' and '1' independently at the output node i , and is expressed as

$$P_0 = \frac{jO_i}{jN_{ij} + jO_{ij}} \quad (10)$$

$$P_1 = \frac{jN_{ij}}{jN_{ij} + jO_{ij}} \quad (11)$$

Where, O_i = logic 1 occurrence at i^{th} node,
 N_i = logic 0 occurrences at i^{th} Node.

Definition: The probability of transition from 0 to 1 or 1 to 0 for a given node of a logic circuit and is defined as

$$SA = P_0 \cdot P_1 = \frac{jO_{ij} \cdot jN_{ij}}{(jN_{ij} + jO_{ij})^2} \quad (12)$$

Estimation of SA of logic gates: The generalized expression to estimate switching activity [3][16] of an elemental logic gate is given by

$$SA = \frac{2^N - 1}{2^{2N}} \quad (13)$$

Where, N represents the number of inputs of the logic gate.

The transition probabilities at each input of basic gates and their switching activities at output node are presented in table I.

Figure 2. Logic diagram of CFA

C. Area (Basic Cell Count)

In this paper, the area of digital arithmetic circuits is defined in terms of basic cell count (number of standard basic logic cells). The basic cell count is one of the logical metrics that are extensively used in estimating the hardware complexity. The area occupied by standard cells from two different libraries is presented in [5].

4. 1-BIT FULL ADDER DESIGNS

A full adder circuit is an arithmetic circuit that performs the addition of three single bit inputs and redirects them to two single-bit outputs. Hence, the full adder is also known as the 3 2 binary adder. In this section, the detailed explanations of three full adder designs are discussed based upon Boolean expressions, logical diagrams, and their switching activities.

A. Conventional Full Adder (CFA) design

Let us consider that three binary inputs are A , B and C_i , that individually indicate the addend bit, augend bit and carry bit Least Significant Bit (LSB) position and produces two binary output bits Sum (S) and Carryout (C). The functional truth table of the full adder [2] module shows the several output values of all attainable input instances represented in table II. The Boolean logic expression for C and S can be obtained from veracity table which is shown

TABLE I. BASIC GATES, INPUT TRANSITION PROBABILITIES AND THEIR SA VALUE

Basic gate	P_0	P_1	SA
AND	$\frac{3}{4}$	$\frac{1}{4}$	$\frac{3}{16}$
OR	$\frac{1}{4}$	$\frac{3}{4}$	$\frac{3}{16}$
NOT	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{4}$

TABLE II. INPUT AND OUTPUT RELATIONSHIP OF 3 2 BINARY ADDER CIRCUIT

A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

in table II in the Sum of Product (SOP) form is given as follows:

$$S = \bar{A}\bar{B}C_i + \bar{A}B\bar{C}_i + A\bar{B}\bar{C}_i + ABC_i \quad (14)$$

$$C_o = \bar{A}BC_i + A\bar{B}C_i + A\bar{B}\bar{C}_i + ABC_i \quad (15)$$

Logic expression (15) can be minimized by using Boolean identity rules and represented as (16)

$$C_o = BC_i + AB + C_iA \quad (16)$$

Figure 2 shows the logic diagram of CFA based on (14, 16) and also specifies the switching activity of each and every output node of logic gates. The CFA requires a total of twenty-two [11 AND, 5 OR, and 6 NOT] basic logic cells, and the total switching activity value of the CFA, which is determined from figure 2 is 3.796. The procedure to estimate the Switching Activity (SA) [7] of conventional full adder is given by

$$SA = \sum_{i=1}^{22} SA_{gate\ i} = 6 \left(\frac{1}{4} + 7 \frac{3}{16} + 9 \frac{7}{64} \right) = 3.796 \quad (17)$$

The block diagram of the m-bit conventional adder consists of m-1 CFAs that are connected in cascaded form, i.e., the output of the first CFA is connected to one of the inputs of the next stage CFA. In m-bit CFA, the output carry bit of the previous stage is interconnected to the input carry bit of the present stage. The SA of present-stage CFA depends on previous stage CFA inputs. The figure 3 shows the block diagram of the m-bit Conventional Adder (CA).

The total switching activity of m-bit conventional adder is an addition of SA of all individual CFA's and is

Figure 3. Block diagram of m-bit CA

represented in (18). The calculation of TSA of m-bit CA is as follows:

$$TSA_{m\ bitCA} = \sum_{i=1}^{X^n} SA_{CFA(i)} \quad (18)$$

Equation (19) indicates the summation of SA of each and every stage for m-bit CA. By applying the generalized method on (19) and it is simplified to (20).

$$TSA_{m\ bitCA} = 6 \left(\frac{1}{4} + 7 \frac{3}{16} + 9 \frac{7}{64} + \dots \right) \quad (19)$$

$$TSA_{m\ bitCA} = \sum_{i=1}^{X^n} \left(\frac{33}{16} + \frac{4}{2^{i+1}} + \frac{9}{2^{i+2}} \right) \quad (20)$$

Furthermore (20) can be simplified as (21) and it represents the generalized formulae for calculation of TSA of m-bit CA i.e. it may be TSA of 8, 16, 32, 64-bit CA.

$$TSA_{m\ bitCA} = \sum_{i=1}^{X^n} \frac{33 \cdot 2^{i-1} + 68 \cdot 2^i + 25}{2^{(i+2) \cdot 2}} \quad (21)$$

The conventional full adder is designed by using twenty two basic standard logic cells, shown in figure 2. The TSBCC of m-bit adder is a summation of the gate count of all individual full adder circuits. The calculation of the

total standard basic cell count needed for the design of an m-bit conventional adder is given by

$$TSBCC_{m\text{-bitCA}} = \sum_{i=1}^{X^n} SBCC_{CFA(i-1)} \quad (22)$$

The gate count of each and every CFA is twenty two. Hence, modify (22) as

$$TSBCC_{m\text{-bitCA}} = 22\ m \quad (23)$$

B. Modified Conventional Full Adder (MCFA) design

The MCFA [11] is designed by redrafting the CFA design logic expressions (14, 16). The modified 1-bit conventional full adder is constituted by three modules as shown in figure 4. Module 1 and module 2 are represented as XOR logic. The module 3, which is a Carry Generation Network (CGN) is used to generate output carry bits. The MCFA design is developed based on intermediate results (denoted as 'P'), which are represented as (24) intermediate signals 'P'. The signal 'P' is defined by taking Exclusive-OR between A and B inputs.

$$P = \bar{A}B + A\bar{B} \quad (24)$$

$$S = \bar{P}C_i + P\bar{C}_i \quad (25)$$

$$C_o = PC_i + AB \quad (26)$$

Figure 4. Block diagram of MCFA

With the help of intermediate results, the sum and carry-out expressions can be attained, and they are represented as logic expressions (25, 26). The switching activity of logic expressions (24, 25) and (26) is specified in figure 5. From the inspection of figure 5 the MCFA requires a total of thirteen [6 AND, 3 OR, and 4 NOT] basic logic cells, and SA is around 2.297. The Switching Activity [18][19] of modified conventional full adder [2] is calculated as follows

$$SA = \sum_{i=1}^{X^3} SA_{\text{module } i} = 4 \left(\frac{1}{4} + 4 \frac{3}{16} + 5 \frac{7}{64} \right) = 2.297 \quad (27)$$

Figure 5. Logic diagram of MCFA

The block diagram of the m-bit modified conventional adder is designed by replacing CFA with MCFA in each and every stage of figure 3. The total switching activity of the m-bit MCA is an addition of the SA of all individual MCFA's, and it shows in (28). The estimation of the TSA of m-bit MCA is as follows:

$$TSA_{m\text{-bitMCA}} = \sum_{i=1}^{X^n} SA_{MCFA(i-1)} \quad (28)$$

While substituting SA values for all stages in (28), it is rewritten as (29). After imposing the generalization method on (29), it becomes (30).

$$TSA_{m\text{-bitMCA}} = 4 \left(\frac{1}{4} + 4 \frac{3}{16} + 5 \frac{7}{64} + \dots \right) \quad (29)$$

$$TSA_{m\text{-bitMCA}} = \sum_{i=1}^{X^n} \left(\frac{28}{16} + \frac{5(2^{i+2}-1)}{2^{(i+2)} \cdot 2} \right) \quad (30)$$

The final expression to calculate TSA of m-bit MCA i.e. 64, 128, 256-bit MCA is given by

$$TSA_{m\text{-bitMCA}} = \sum_{i=1}^{X^n} \frac{28 \cdot 2^{2i} + 20 \cdot 2^i - 5}{2^{(i+2)} \cdot 2} \quad (31)$$

Equation (31) represents the generalized expression, which is used to estimate the TSA of m-bit MCA and it is also applicable for multi-operand adders.

The modified conventional full adder is designed by using thirteen basic standard logic cells shown in figure 5.

The calculation of the total standard basic cell count needed for the design of an m-bit modified conventional adder is given as

$$TSBCC_{m\text{-bitMCA}} = \sum_{i=1}^{X^n} SBCC_{MCFA(i-1)} \quad (32)$$

Each and every MCFA requires thirteen gates. As a result,

(32) becomes

$$TSBCC_{m \text{ bitMCA}} = 13 m \quad (33)$$

[14][16] of PFA is calculated as follows:

$$SA = \sum_{i=1}^X SA_{\text{module } i} = 4 \left(\frac{3}{16} + 5 \frac{7}{64} \right) = 1.297 \quad (37)$$

C. Proposed Full Adder (PFA) design

The Exclusive-OR gate (XOR) behaves as one of the fundamental modules used in binary adder circuits. The functionality of the XOR gate is derived by using three basic gates (AND, OR, and NOT). The conventional XOR gate shown in figure 6 requires five basic gates and an SA value of 1.065. The proposed XOR gate is designed by applying the logic decomposition method to a conventional XOR gate.

The block diagram of the m-bit proposed conventional adder is designed by replacing CFA with PFA in each and every stage of the figure 3. The total switching activity of m-bit PA is an addition of the SA of all individual PFA's and is expressed as (38). The estimation of the TSA of m-bit PA is as follows:

$$TSA_{m \text{ bitPA}} = \sum_{i=1}^X SA_{PFA(i)} \quad (38)$$

Equation (39) represents the sum of the SA values of each and every stage, which is designed by using the proposed full adder.

$$TSA_{m \text{ bitPA}} = 4 \left(\frac{3}{16} + 5 \frac{7}{64} \right) \quad (39)$$

Figure 6. Logic diagram Conventional and Proposed XOR gate

In proposing the XOR gate, it is possible to obtain a minimum SA value and basic logic cells by removing two NOT gates without changing the functionality of the XOR gate. The proposed XOR gate is designed with three gates and the SA value is reduced to 0.5625. Using the proposed XOR gate, a new full adder is developed and it is shown in figure 7. The proposed 132 binary adder is designed based upon the following Boolean expressions:

$$P = (\bar{A} + \bar{B})(B + A) \quad (34)$$

$$S = (\bar{P} + \bar{C}_i)(C_i + P) \quad (35)$$

$$C_o = PC_i + BA \quad (36)$$

After applying the generalized method on (39), it can be rewritten as (40).

$$TSA_{m \text{ bitPA}} = \sum_{i=1}^X \left(\frac{12}{16} + \frac{5(2^{i+2}-1)}{2^{(i+2)^2}} \right) \quad (40)$$

The final equation to estimate the TSA of any size m-bit PA is represented by (41) and is represented as

$$TSA_{m \text{ bitPA}} = \sum_{i=1}^X \frac{12 \cdot 2^{2i} + 20 \cdot 2^i + 5}{2^{(i+2)^2}} \quad (41)$$

The proposed full adder is designed by using nine basic standard logic cells shown in figure 7. The calculation of the total standard basic cell count needed for the design of the m-bit proposed adder is given by

$$TSBCC_{m \text{ bitPA}} = \sum_{i=1}^X SBCC_{PFA(i)} \quad (42)$$

Each and every PFA requires nine gates. Hence, (42) becomes

$$TSBCC_{m \text{ bitPA}} = 9 m \quad (43)$$

Figure 7. Logic diagram of PFA and SA value at each output node

Based on the logic decomposition method, the Boolean logic expressions (24, 25) are modified as logic expressions (34, 35). The logic diagram of the proposed full adder is shown in figure 7. The PFA has nine (4 AND, 3 OR, and 2 NAND) basic cells, and the SA value is 1.297. The SA

The overall comparison of all three adders in terms of basic logic (AND, OR, NOT) cells, standard basic cell count, and switching activity value is presented in table III. From table III (* is a NAND gate), it can be observed that the proposed method has a minimum basic cell count and an SA value.

Here, the SA value of a particular bit adder is estimated from (21, 31 and 41). First, we calculated the SA value for (2-16) bit adders and then (17-128) bit adders. Furthermore,

TABLE III. THEORETICAL COMPARISON OF THREE FULL ADDERS

Type of Adder	AND Cells	OR	NOT	SBCC	SA
CFA	11	5	6	22	3.796
MCFA	6	3	4	13	2.297
PFA	4+2*	3	0	9	1.297

TABLE IV. AVERAGE SA VALUE OF M-BIT ADDER AT ANY PARTICULAR BIT

Type of m-bit Adder	CA	MCA	PA
At (2-16)-bit	2.296	1.822	0.822
At (17-128)-bit	2.063	1.75	0.75

an average SA value is estimated for all m- bit adders. Byrequires nine basic logic cells, 7.15ns of delay, and 282mW inspection of SA values presented in table IV, we foundof power dissipation. that m- bit PA requires a lower SA value.

5. RESULTS AND COMPARISON

In the following section, we rst discuss the imple- mentation results, followed by a performance comparison, and followed by theoretical analysis to verify the simulation results.

The power dissipation, delay, and RTL schematic of the PFA are shown in gure 10. By investigating the implementation result of the PFA, the PFA corresponds to seven basic logic cells, 211mW of power dissipation, and 7.106ns of delay.

In this work, we used three different full adder designs. The three presented designs are evaluated based on performance metrics such as cell count, power dissipation, and delay. The entire motif has been evolved using Verilog HDL and implemented in Xilinx Vivado V.2017 under the Zynq-7000 family. The RTL diagrams of the presented designs are obtained using the Open Elaborated Method. The RTL schematic, power dissipation, and delay of CFA are shown in gure 8. According to the CFA implementation result, the CFA is associated with seventeen basic logic cells, 387mW of power consumption, and a delay of 7.125ns.

The power dissipation of three! 32 binary adder designs at different load capacitances (i.e., 3pF, 6pF, 12pF, and 15pF) is observed and shown in gure 11. At any load capacitance, the proposed full adder has minimum dynamic power dissipation.

Figure 8. Implementation result of CFA

Figure 10. Implementation result of PFA

Figure 9. Implementation result of MCFA

Figure 11. The power dissipation of full adder designs at different load Capacitance (CL)

The delay, power consumption, and basic logic cell count of MCFA is shown in gure 9. In view of the synthesis and implementation results of MCFA, the MCFA

The results of various full adders in terms of the standard basic cell count, power, and delay after synthesis and

TABLE V. COMPARISON OF BINARY ADDERS BASED ON IMPLEMENTATION RESULTS

Name of the Design	SBCC	Signal Power	Logic Power	Dynamic Power(mW)	Static Power(mW)	Delay (nsec)
CFA	17	4	1	264	123	7.125
MCFA	9	2	1	160	122	7.125
PFA	7	1	< 1	90	121	7.106

TABLE VI. COMPARISON OF BINARY ADDERS BASED ON PERFORMANCE METRICS

Name of the Design	Delay (nsec)	Average Power	Dynamic Power	FOM (nJ)	PDP (nJ)	EDP (10 ²¹ J)
CFA	7.125	193.5	264	1.378	1.881	13.402
MCFA	7.125	141	160	1.004	1.140	8.122
PFA	7.106	105.5	90	0.749	0.639	4.544

implementation using the Zynq-7000 family from figures 8, 9 and 10 are taken to evaluate the performance metrics of adder designs. The performance matrices of three 3! 2 binary adder designs are compared in terms of the standard basic cell count, critical path delay, and power dissipation shown in table V. From the implementation results of three adder designs, we found that PFA requires a minimum standard basic logic cell count, power dissipation, and delay compared to the other two designs.

Further, we can estimate other performance metrics such as Figure of Merit (*FOM*), *PDP*, and *EDP*. *FOM* of digital IC is defined as the product of critical path delay and average power dissipation. It is a term used to distinguish the performance of digital logic circuits. In any digital circuit, a low value of *FOM* is desirable.

$$FOM = CPD \cdot P_{avg} \quad (44)$$

Because power dissipation and delay alone cannot assess the overall performance of an adder circuit, Power Delay Product (*PDP*) is defined as the product of dynamic power consumption and Critical Path Delay (CPD) and is expressed as

$$PDP = P_d \cdot CPD \quad (45)$$

In order to design a high-speed and performing full adder, we need an optimized CPD and PDP value. However, a logic circuit with small values of *PDP* may execute slowly. Therefore, an energy delay product (*EDP*) is calculated to comment on the high performance of the logic circuit. It is a product of PDP and CPD. Thus, *FOM*, *PDP*, and *EDP* have been calculated for the full adder designs and are shown in table VI. Figure 12 shows a graphical representation of the proposed full adder in terms of percentage improvement in reduction of total standard basic cell count, *FOM*, *PDP*, and *EDP* with respect to conventional and modified conventional full adders. The signal and logic power dissipation of the proposed full adder after implementing the design using the Xilinx Vivado tool is 3 mW and the power dissipation reported by the simulation tool is verified by using theoretical analysis. The theoretical analysis is done on the

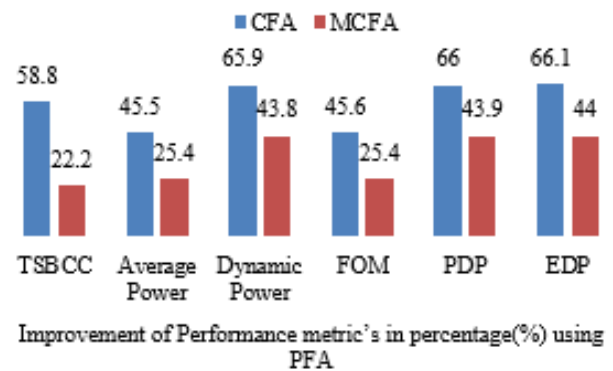


Figure 12. Percentage of improvement in the performance metrics of PFA compared to others

Register Transfer Level (RTL) schematic of the proposed full adder. Here we performed a theoretical analysis on the proposed full adder only and this method is applicable for the remaining designs. In order to evaluate the dynamic (signal and logic) power dissipation, we need to know the switching activity and load capacitance of each and every gate. The Fan-out (*F*) concept is used to find the load capacitance of any logic gate. Fanout is defined as the ratio of load capacitance and to the gate capacitance.

$$F = \frac{C_L}{C_G} \quad (46)$$

Where, C_L indicates the load capacitance of the gate,

F represents Fanout,

C_G denotes the gate capacitance of the gate.

From the equation (46) the load capacitance is expressed as

$$C_L = F \cdot C_G \quad (47)$$

The load capacitance and switching activity at each node in the RTL schematic are listed in table VII. While calculating dynamic power dissipation, we considered some specifications of the Zynq-7000 family. According to the

TABLE VII. THE SA VALUE AND LOAD CAPACITANCE AT OUTPUT NODE OF EACH AND EVERY GATE FOR FIGURE 10

Node	1	2	3	4	5	6	7
SA	$\frac{3}{16}$	$\frac{3}{16}$	$\frac{3}{16}$	$\frac{7}{64}$	$\frac{7}{64}$	$\frac{7}{64}$	$\frac{7}{64}$
C_L	C_G	$2C_G$	$2C_G$	C_G	$2C_G$	C_G	C_G

TABLE VIII. I/O POWER CONSUMPTION CALCULATIONS FOR FIGURE 10

S.No	I/O path	Nodes	SA value	Pd@(2.2V,9pf,140MHz)
1	A! S	[2,3,5,6],[1,3,4,6],[2,3,4,6], [1,3,5,6]	4.0938	27.286
2	A! C_Y	[1,3,5,7],[2,7],[2,3,5,7]	2.4531	16.350
3	B! S	[2,3,5,6],[1,3,4,6],[2,3,4,6], [1,3,5,6]	4.0938	27.286
4	B! C_Y	[1,3,5,7],[2,7],[2,3,5,7]	2.4531	16.350
5	C! S	[4,6],[5,6]	0.5469	3.645
6	C! C_Y	[5,7]	0.3281	2.186

Xilinx Vivado tool, the total power dissipation consumed by the circuit is defined as the sum of signal, logic power, and input to output power.

$$P_D = P_{SL} + P_{IO} \quad (48)$$

Where, P_D represents total dynamic power dissipation, P_{SL} is power dissipation due to signals and logic, P_{IO} is power dissipation due to transmission of data from input to output.

The I/O power consumption calculation for each and every combination of input signal to output signal is shown in table VIII and the total I/O power is **85mW**.

$$P_{SL} = \sum_{i=1}^{N_{de}} [C_{Li} V_{dd}^2 f] \quad (49)$$

$$P_{SL} = \left(\frac{3}{16} C_g + \frac{3}{16} 2C_g + \frac{3}{16} 2C_g + \dots \right) V_{dd}^2 f \quad (50)$$

$$P_{SL} = 3 \text{ mW} \quad (51)$$

From equation(51) and table VIII the total dynamic power consumption is **88 mW**. According to implementation results of the PFA design, the total dynamic power dissipated by the PFA design is **90 mW**, which is verified by theoretical dynamic power calculation analysis.

Furthermore, the three full adder design methods are imposed on 32-bit adders and compared in terms of total standard basic cell count. The proposed adder design reduces the total standard basic cell count compared to the remaining adder designs, which is shown in table IX. The generalized expression to estimate the total standard basic cell count for any size of adder is shown in table X.

Using the values listed in table X, further, we are defining other performance metrics such as Figure of Merit (FOM), PDP, and EDP. The performance metrics of the 32-

bit adder design are shown in table XI. The improvement of 32-bit proposed adder performance metrics in terms of percentage with respect to 32-bit CA and MCA is shown in figure 13. The proposed 32-bit adder is attractive in improving 59.1% in theoretical TSBCC, 58.8% in RTL TSBCC, 57.7% in dynamic power dissipation and 60% in PDP compared to conventional method and 30.8% in theoretical TSBCC, 22.2% in RTL TSBCC, 50.7% in dynamic power dissipation and 52.9% in PDP compared to the modified conventional method. The EDP of the proposed 32-bit adder is reduced by 62.2% compared to the conventional method and 55.1% compared to the modified conventional method.

The simulation result of 1-bit adder when all inputs are

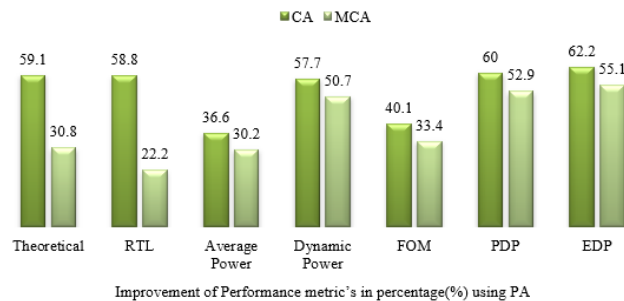


Figure 13. Performance metric's improvements in 32-bit PA w.r.t CA and MCA

logic1 is shown in figure 14. The 32-bit adder is simulated by applying A = 4b9 and B = 11d5 as inputs, which results output as 'Z = 168e'.



Figure 14. Simulation result of 1-bit and 32-bit adder



TABLE IX. IMPLEMENTATION RESULTS OF 32-BIT ADDER

Name of the Design	Theoretical TSBCC	RTL TSBCC	P_{SL}	P_{static}	Delay (nsec)
CA	704	544	156	150	24.81
MCA	416	288	134	144	24.56
PA	288	224	66	128	23.45

TABLE X. COMPARISON OF M-BIT ADDERS w.r.t CELL COUNT

m-bit	Theoretical	RTL
CA	22 m	17 m
MCA	13 m	9 m
PA	9 m	7 m

TABLE XI. 32-BIT ADDER, PERFORMANCE METRICS COMPARISON

Name of the Design	Delay (nsec)	Average Power	Dynamic Power	FOM (nJ)	PDP (nJ)	EDP (nJ)
CA	24.81	153	156	3.795	3.870	96.01
MCA	24.56	139	134	3.413	3.291	80.83
PA	23.45	97	66	2.274	1.547	36.29

CONCLUSION

Based on the switching activity and logic decomposition methods, a novel full adder is proposed. The SA values of basic logic gates are compared, and the NOT gate requires a large SA value. In proposing full adder, we reduced the count of NOT gates, which eventually leads to minimize the dynamic power dissipation and standard basic cell count. The proposed full adder shows significantly better performance in terms of the standard basic cell count, power dissipation, FOM, and EDP respectively, compared to the other two designs. However, the proposed full adder does not dissipate the minimum power (which is applicable for future scope of research work), it has the minimum logic cell count and better EDP compared to the other two adder designs. Thus, the proposed full adder is suitable for large bit size adders, multipliers, and FinFET based VLSI digital circuits and architectures.

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