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Design of Compensated Supply Circuit Topology for a Ring Oscillator

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Abstract: In an era of digitalization, a precise, accurate and portable feature is the prime concern of any gadget in the market. The accuracy of any design depends on supply variation, circuit methodology and environmental upshots. This paper propose a compensated supply circuit topology using PTAT and CTAT techniques for a ring oscillator as modern data converter architecture application. In this circuit, an appropriately weighted threshold voltage of diode (VTHP, VTHN) helps provide a constant voltage when supply voltage varies from 1.6 to 5volt. To compensate the temperature variation which varies from (-50 to 130^0C) that will be acquired through the help of complementary to absolute temperature (CTAT) and be proportional to absolute temperature (PTAT) voltage. With the help of a high speed low dropout voltage regulator, the output of the proposed circuit becomes adaptive. It can significantly reduce the power dissipation with respect to uncompensated supply circuit. It is implemented on Cadence Virtuoso with 65-nm CMOS technology, the simulation results of ring oscillator have verified the success of PVTCS where a ring oscillator works as the load of the circuit which shows a high frequency oscillation at 413.8MHz and reduces the power consumption by 72.25 % with 42.6 % better proportional speed. In this paper, Monte-Carlo analysis for power dissipation and corner analysis are carried out for the proposed circuit.These simulations show the stability of the proposed circuit. Layout of the proposed circuit is designed on 65-nm CMOS technology.

Keywords: Cadence Virtuoso, Ring oscillator, Differential amplifier, Low dropout voltage regulator, Diode, Proportional supply voltage and temperature compensation, Monte Carlo analysis, Process Corner analysis

1. Introduction

A Digital electronics circuit has two well-known problems- first, supply variation of the digital circuit and second, temperature variation by the environmental affect [1], [2]. Digital circuits like smart phone, smart watch, laptop and many more are easy to handle, they face temperature and supply variations which can directly affect the output of the circuit. Many Very Large Scale Integration (VLSI) circuit designers work to address this problem. Some designers have given an idea of "Body Bias Technique" [3], [4] that compensates the effect of supply variations, but it increases the power dissipation of the circuit drastically. Some of them gave the idea of "mixed body bias with fixed threshold voltage and drain current"[5] that compensated the input supply variation; but in the point of temperature variation, compensation is not too affected very much. Lastly,there was an idea of a "proportional supply voltage and temperature compensated supply circuit" that compensates both supply and temperature variations. A (PVTCS) circuit forms with the help of current mirror and p/n type diode [6], [7], [8], [9], [10], [11]. When a current source passes through a diode it behaves as complementary to absolute temperature (CTAT) [12]. As the temperature increases, the voltage across the diode decreases. Research in energy efficient high-performance computing (HPC) continues to be driven by both environmental and cost-related factors. The investigations can be broadly divided into three main focus areas: compiler and runtime optimizations; operating system automations; and power efficient microprocessor design. In order to validate HPC energy efficient compiler/runtime optimizations, the key challenge lies in precisely measuring thread-specific energy consumption and the corresponding impact of code-level optimizations.

$$I_S = bT^{4+m}exp^{-Eg/KT} \tag{1}$$

$$(I_S)/T = b(4+m)T^{3+m}exp^{-E_g/kT} + bT^{4+m}(exp^{-Eg/kT})(E_g/kT^2) \tag{2}$$

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Where q is charge, I_S represents the saturation current in equation (1), K represents Boltzmann's constant. Equation (2) defines as the saturation current variation with respect to temperature. The diode voltage VD is depicted in equation (3).

$$V_D = V_T ln(I_D/I_S) \tag{3}$$

$$(V_D)/T = (V_T)/T ln I_D/I_S - V_T/I_S(I_S)/T \tag{4}$$

Where VD is diode voltage and VT is the thermal voltage, in equation (4) the partial differentiation of the diode voltage with respect to temperature that will show the negative slope as the temperature increases, that is known as CTAT voltage. To compensate that voltage, we use another voltage variation named as proportional to absolute temperature (PTAT) voltage [13] that will form by the difference of two diode voltage. Combination of CTAT and PTAT voltage that will form a reference voltage which will not affect with supply and temperature variation. The reference voltage provides a noise with respect to temperature variation, to overcome that noise a differential amplifier circuit introduce that can eliminate the noise effect as well as provide a stability to the circuit [14], [15], [16], [17]. The differential amplifier (DA) gives the output in the sinusoidal form so that a high speed low dropout voltage regulator circuit helps to provide a constant voltage at load of the circuit. The low dropout (LDO) voltage regulator helps to compress the fluctuation of input voltage and gives a constant voltage to the load [18], [19], [20], [21], [22], [23]. At the load side we use a ring oscillator circuit that form by the twenty-one inverter with similar (W/L) ration which will help to provide better performance. BiCMOS based temperature compensation topology is used to suppress the effect of the temperature variation on the supply of the load [24]. In [25] a CMOS technology a stable voltage is provided that has wide range of temperature variation. One more bandgap reference circuit (BGR) is implemented in [26] with the use of a single BJT branch and a PTAT based amplifier. Cascade Miller frequency compensation technique is used in the amplifier circuit used for the band gap reference. In [27] compensation circuit is designed which increases the voltage accuracy with a wide temperature range. This circuit consists of addition circuit, subtraction circuit and current mirror circuit. For reducing Analog single-event transient radiation effects, three band gap circuit is used [28]. To find exact current and voltage reading for find out the exact position of automotive battery. In [29] a BGR circuit is implemented which has digital calibration technique. An accurate current mode BGR [30] is designed which contain two operational amplifiers that uses to generate PTAT and CTAT current sources. This BGR has shared offset compensation technique for its amplifiers. At the low voltage operation many circuit parameters are effected by the process, voltage and temperature variations[31]. To reduce this problem a compensating circuit which used the variable current source to control the bias potential for the Low noise amplifier [32].

In the figure 1 block diagram of PVTCS first block represent as current mirror circuit that fed a constant current to p/n type diode that will form a reference voltage but it has some noise, to overcome that problem a differential amplifier circuit introduce that can compress the noise effect and provide high stability to the circuit. After that for regulated output a high speed low dropout voltage used that eliminate fluctuation of the input and provide a constant voltage to ring oscillator circuit that behave as a load of the circuit.

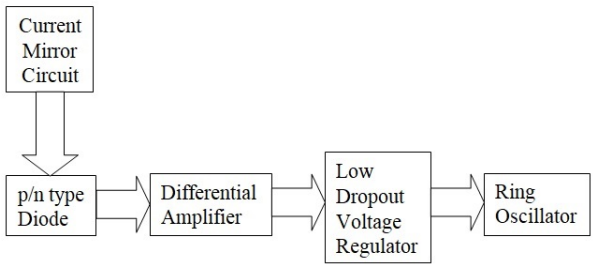

Figure 1. Block Diagram of PVTCS with ring oscillator

Compensated supply topology for a ring oscillator is implemented in this work. Section II describes the mathematical analysis and temperature Variation Compensation. Discussion of proposed work is in Section III. Section IV represents the result and discussion of the proposed work with process corner analysis, Monte Carlo analysis and the layout of the proposed design. The proposed work is evaluated against conventional circuits considering parameters such as power, proportional variation, temperature variation and supply variation. Section V is the overall conclusion of the proposed work.

2. MATHEMATICAL ANALYSIS

A current mirror in figure 2 provides a constant current and that constant current passes through the diode behave as CTAT and different of two CTAT voltage works as a PTAT voltage. Equations (7) and (8) are the drain current which defines in different branch.

$$V_{01} = g_m r_{01} V_{gs3} \tag{5}$$

Where Vgs3 in equation (5) is expressed in equation (6).

$$V_{gs3} = V_1 - V_{01} \tag{6}$$

$$I_{D1} = \frac{1}{2}\mu_n C_{OX}(w/l)_1(V_{gs} - V_{th})^2(1 + \lambda V_{ds})_1 \tag{7}$$

$$I_{D1} = \frac{1}{2}\mu_n C_{OX}(w/l)_2(V_{gs} - V_{th})^2(1 + \lambda V_{ds})_2 \tag{8}$$

Equation (9) is the division of equation (7) with equation

(8).

$$\frac{I_{D2}}{I_{D1}} = \frac{(w/l)_1}{(w/l)_2}\frac{(1+\lambda V_{ds})_1}{(1+\lambda V_{ds})_2} \tag{9}$$

$$V_{out} = V_{01}\left[1 + \frac{I_1 + V_2(r_{03}R_3)/(r_{03}+R_3)}{R_{d2}(I_2 - I_{ref})}\right]\frac{(r_{03}R_3)}{(r_{03}+R_3)} - V_1\frac{(r_{02}R_{d1})}{(r_{02}+R_{d1})} \tag{10}$$

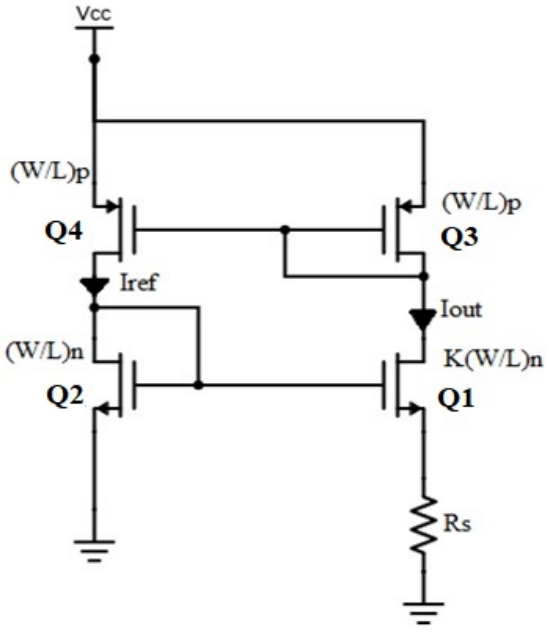

Figure 2. Current Mirror Circuit

The output voltage of current mirror circuit represents in equation (10).

By the above equation, we can determine that the output voltage is related on different parameters like as source resistance RS, output resistance ro, drain resistance Rd and reference current Iref. The overall output voltage Vout in term of the reference voltage and reference current is defined. Further, this design can be used to implement Proposed reference circuit for providing a constant current in each branch and reward the effect of supply and temperature variation in this work. A reference voltage forms with the help of CTAT and PTAT voltage that describes below with equations.

A. *Temperature Variation Compensation*

As a constant current passes through the pn-junction diode, it provides a negative temperature coefficient voltage. The basic equation of diode current is $I_D = I_S$ exp (V_D/V_T) where thermal voltage is (V_T). Saturation current (I_S) is directly relative to mobility, temperature and intrinsic carrier concentration of silicon. The mobility μ is define as ${}_oT^m$, where m-3/2, and intrinsic carrier concentration is $n_i{}^2T^3\exp(-E_g/KT)$, where E_g is energy bandgap of silicon and its value is 1.12eV. The diode equation $V_D = V_T\ln(I_D/I_S)$ provides a negative slope by the I_S dependence on temperature. Therefore,

$$\frac{V_T}{I_S}\frac{I_S}{T} = (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2} \tag{11}$$

By the further solving of the equation (11), it is expressed in equation (12).

$$\frac{V_D}{T} = \frac{V_T}{T}ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T \tag{12}$$

Equation (4) gives temperature coefficient (T_C) of the diode voltage at given temperature (T), and it provides $\delta V_D/V_T$ -1.5 mV/K. Figure 3(a) and 3(b) represents positive temperature coefficient and negative temperature coefficient respectively.To compensate the adverse voltage, a constructive voltage will be obtained with the help of PTAT. PTAT voltage forms by the subtraction of two CTAT voltages that mathematically eliminate the saturation current dependency with diode voltage. In the PTAT diode, voltage only depends on thermal voltage that is directly related to temperature as the temperature increases, PTAT voltage will increase too. The difference between Positive temperature coefficient (PTC) and Negative temperature coefficient (NTC) voltage circuit is given in equation (13) and (14).

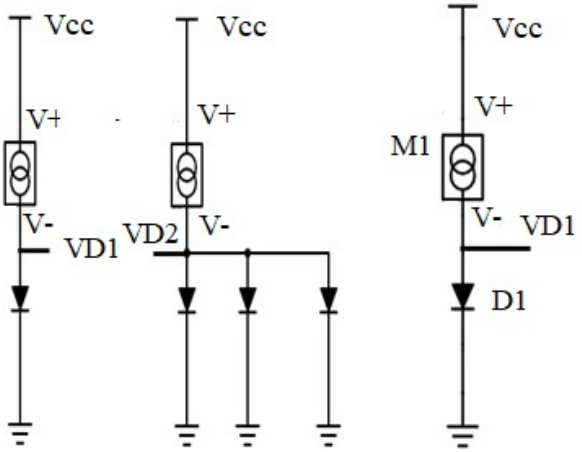

Figure 3. (a). PTC (b). NTC

$$V = V_{D1} - V_{D2} \tag{13}$$

$$= V_T ln(nI_0/I_{S1}) - VT ln(I_0/I_{S2}) = V_T ln(n) \tag{14}$$

The combination of CTAT and PTAT voltage provides a constant voltage which will not be much affected too much because of supply and temperature variations. By the simulation of above circuit, we observed that supply voltage should have proper voltage to compensate the temperature variations. As the adjustment of temperature compensation delay of the circuit independent of the temperature variation.

$$t_d = \left[\frac{1}{2} - \frac{(1-(V_{TH}/(V_{DD}))}{1+\alpha}\right] t_T + \frac{C_L V_{DD}}{I_D} \qquad (15)$$

where t_d in equation (15) represents the delay of the circuit and velocity saturation index represented as α and I_D is the drain current of the MOSFET. $I_D = \beta(V_{GS}-V_{TH})^{\alpha}$ where $\beta = (1/2)\mu(T)C_{OX}(W/L)$

$\mu(T)$ is defined as the mobility of electron or hole where T represents as operating temperature, and C_{OX} is gate oxide capacitance. By the above expressions, equation (15) is modified as equation (16).

$$t_d = \frac{C_L V_{DD}}{2\beta(V_{DD}-V_{TH})^{\alpha}} \qquad (16)$$

3. PROPOSED CIRCUIT

A. Proposed Reference Circuit

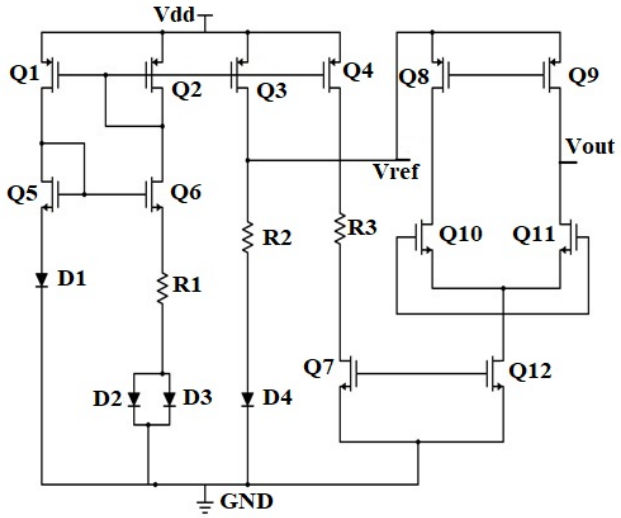

Figure 4. Proposed Reference Circuit

In this paper, ring oscillator reference circuit with PTAT and CTAT techniques(proposed design) reference circuit are designed to provide a constant supply to the digital load circuit while input supply and temperature of the circuit contrast. By this circuit, digital circuit output does not fluctuate with supply and temperature variation. In the given figure 4, proposed reference circuit is shown where transistor Q1, Q2, Q3, Q4, Q5 and Q6 work as basic current mirror circuit and diode D1. It may be p/n type for the perfect VTHN and VTHP threshold voltage. By the help of diode D1, form a diode voltage VD, it behaves as complementary to absolute temperature.

TABLE I. Transistor Parameter

Transistor	$\mu Cox(\mu A/V^2)$	W/L(nm/nm)	β	Vth
NMOS	48.6	1800/180	241	0.38
PMOS	29.08	5400/180	460	0.37

Table I represents the transistor parameters used in the proposed reference circuit. With the help of resistance R1, equate the voltage VD1 and voltage across D2 and D3. So that it can be obtained proportional to absolute temperature for the compensation of temperature and supply voltage. A current mirror circuit provides a constant current in each branch so that the resistance value is easily calculated. After that a constant reference voltage is fed as an input supply to the differential amplifier to avoid noise effect as well as improve the stability of the circuit. As the gain of the differential increases the output of the differential is improved with the difference of the input voltage.

B. Low DropOut Voltage Regulator Circuit

As shown in figure 4, it can be easily understood that the output of the differential amplifier is fed as an input of the low drop-out (LDO) voltage regulated circuit. The LDO voltage is a regulated circuit to eliminate the fluctuation which is obtained by differential amplifier. In the low drop-out voltage regulator, we used input and output capacitance 1μF and 10μF respectively. The major part of the low drop-out voltage regulator circuit is error amplifier which compares the input reference voltage and differential amplifier voltage. The error amplifier output is fed into PMOS gate terminal, in which drain terminal behaves as an output of the low drop-out voltage regulated circuit.

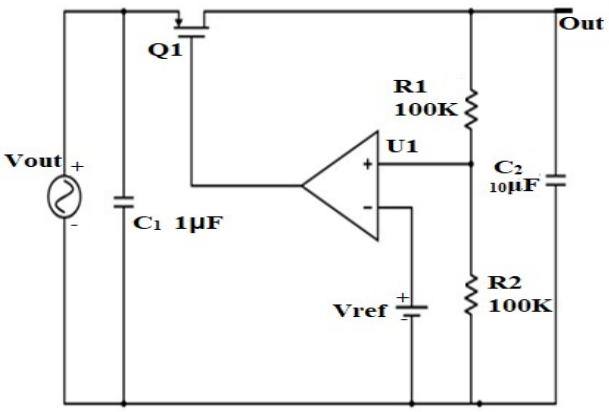

Figure 5. Schematic of LDO Circuit

Figure 5 shows the LDO circuit where Op Amp behaves as error amplifier and positive terminal of the error amplifier

and it's positive terminal is taken as half of the output voltage Vout which is output of differential amplifier. By the comparison of Vout and Vref voltages, it provides a minimum output voltage which behave as gate terminal voltage of the PMOS transistor. The minimum voltage found in the error amplifier define the difference of output voltage as much input voltage. In this circuit, both active and passive components are used like resistors capacitors and Op Amp is used for the purpose of filtering. Low-dropout (LDO) regulators are similar to the linear voltage regulator.

C. Ring Oscillator

To represent the validation of proposed PVTCS a digital load oscillator is investigated. In this paper, ring oscillator is used as a load, which has twenty-one inverters. In the given figure 6, the out terminal is the supply of the ring oscillator which comes from the high speed LDO circuit. Since the Out supply is unaffected with supply and temperature variations, it will also be unaffected the inverter chain output from supply and temperature variations. The oscillation frequency of load is simulated under supply and temperature variations provided in the range of megahertz.

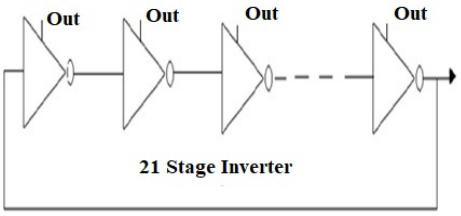

Figure 6. Schematic of Ring Oscillator Circuit

D. Process Supply Voltage and Temperature Compensated Circuit with Ring Oscillator

Figure 7. represents a reference circuit that forms by the mathematical calculation of PTAT and CTAT techniques, to avoid the common mode of the circuit and improve the gain of reference voltage use a differential amplifier, to regulate the voltage and provide a constant voltage to point a load of digital circuit that define as ring oscillator. The output waveform of compensated circuit gives a smooth oscillation and this occurs due to constant supply reach for digital load circuit. The ring oscillator design with twenty-one inverters have similar aspect ratio of W/L. This will help in achieving proper oscillation at output side. Frequency of the ring oscillator is 412.8 MHz, this is large in range as compare to previous work.

4. RESULT DISCUSSION AND ANALYSIS

The validation of the circuit is simulated on CADENCE software. The schematic of proposed proportional supply voltage and temperature compensated circuit is designed with the help of 65nm CMOS technology. As discussed in proposed work, the circuit waveform behaves similarly. The simulation of proposed circuit is depicted in figure 8. In the figure 8 y-axis represents as input, reference voltage and Vout where x-axis represents as dc voltage.

As dc voltage increases from 1.6 to 5 volt, the reference voltage provides 0.7 volt approximately. Vout represents as differential output voltage and it also follows the reference voltage properly. In the figure 8, waveform represents as reference voltage on y-axis and voltage variation on x-axis. By the differential amplifier circuit behavior of reference voltage is not constant; there is fluctuation in the output. When this output is passed through an LDO circuit, the fluctuated output voltage comes under constant voltage range. from the figure 8 the input waveform of the LDO circuit provides high fluctuation from 1.5 to 0.5 volt. Actually, this input waveform is the differential amplifier circuit's output. After the LDO circuit operation, the output of the LDO circuit compresses the input voltage and provides an approximate 0.9 volt at LDO output terminal that behaves as an input for the ring oscillator circuit. The full schematic circuit is represented in figure 7 in the form of symbol and each symbol holds own circuit internally.Figure 9 depicts the simulation waveform of the proposed reference circuit with respect to temperature variation. In the figure 9, waveform is represented as reference voltage on y-axis and temperature variation on x-axis. The figure 8 gives the idea of output of the proposed reference circuit is mostly constant with the variation in the input DC voltage to the circuit and figure 9 gives the behavior of the proposed reference circuit with change in the temperature. The output of the proposed reference circuit is constant with respect to the variation of the change in the voltage supply and temperature. During this time, the input of the proposed reference circuit is kept constant. Figure 10. represents the overall output of PVTCS circuit that includes ring oscillator output also. Figure 11. represents the behaviour of the PVTCS circuit with different temperature. Table II represents reference voltage variation w.r.t. input dc voltage, this shows the Vout is nearly unfluctuated with change in input Vdc of the proposed circuit. Table III represents output voltage variation w.r.t. temperature variation. Table IV represents the comparison of previous work in PVT circuit. The parameters are technology, power dissipation, body biased, proportional variation and temperature variation. Layout area of this paper is more as compared to previous work but it gives better result in supply and temperature variation.

TABLE II. Reference and Output Voltage w.r.t. Input Supply Variation

Vdc(V)	Vref(V)	Vout(V)
1	0.422	0.146
2	0.729	0.160
3	0.755	0.163
4	0.792	0.166
5	0.803	0.173

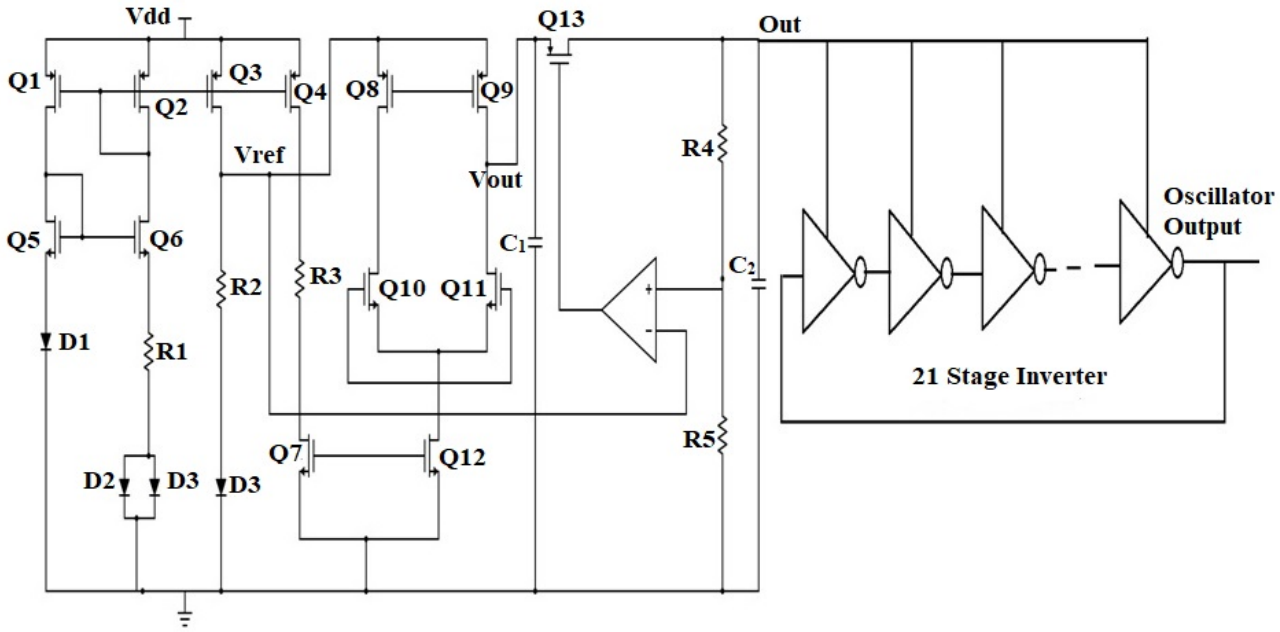

Figure 7. Schematic of PVTCS circuit with ring oscillator

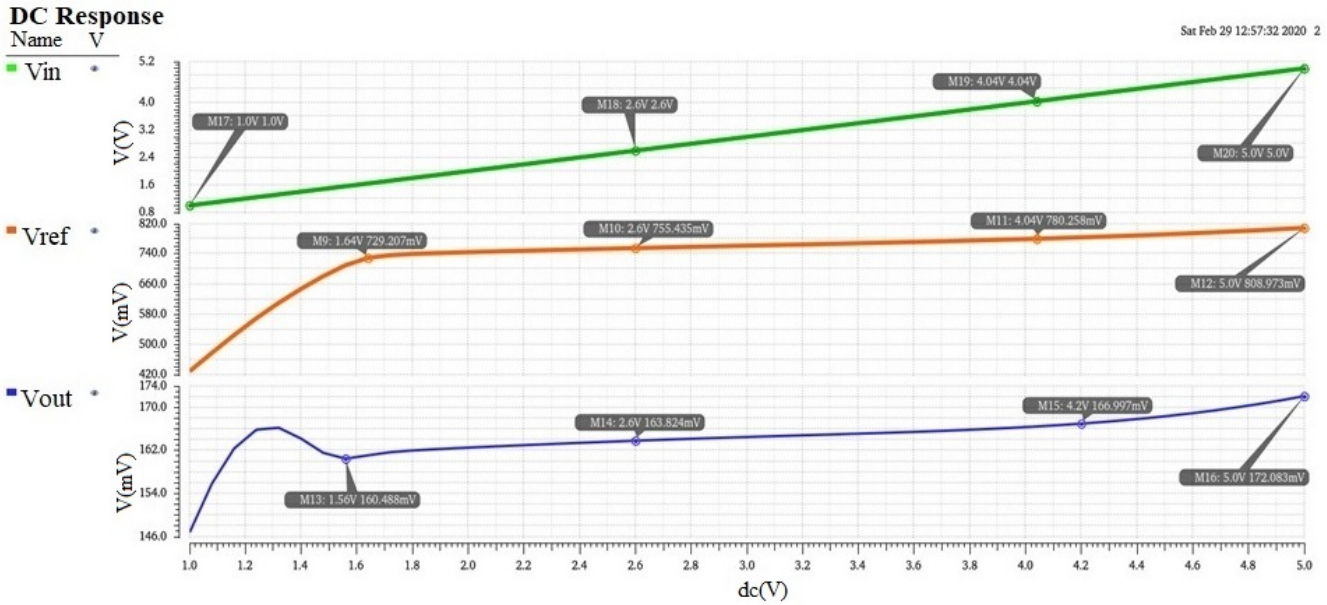

Figure 8. Simulation waveform of Proposed Reference Circuit w.r.t. dc voltage

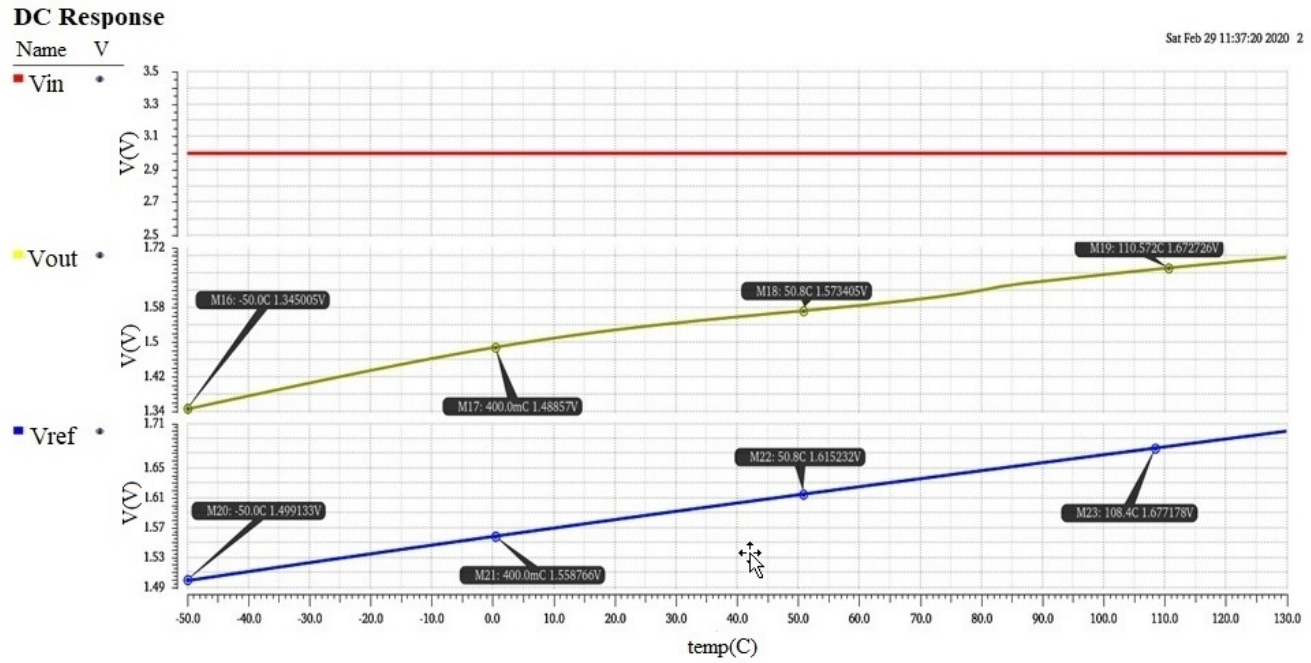

Figure 9. Simulation waveform of Proposed Reference Circuit w.r.t. temperature

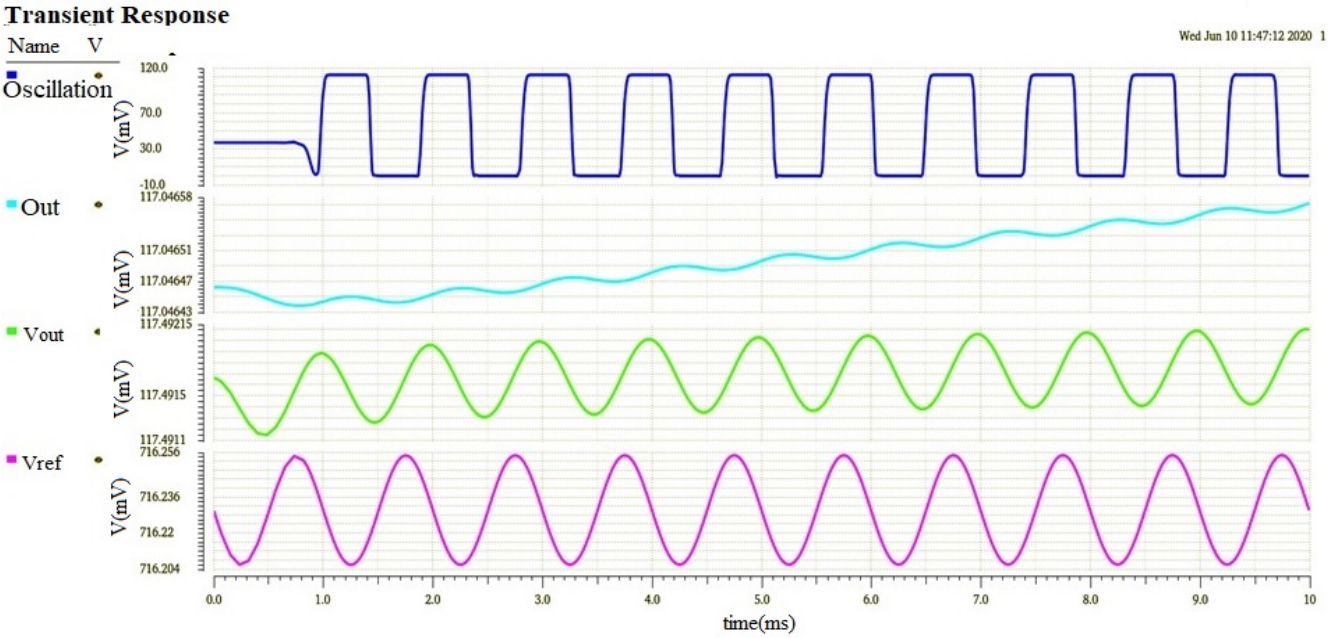

Figure 10. Simulation waveform of Proposed Reference circuit with ring oscillator

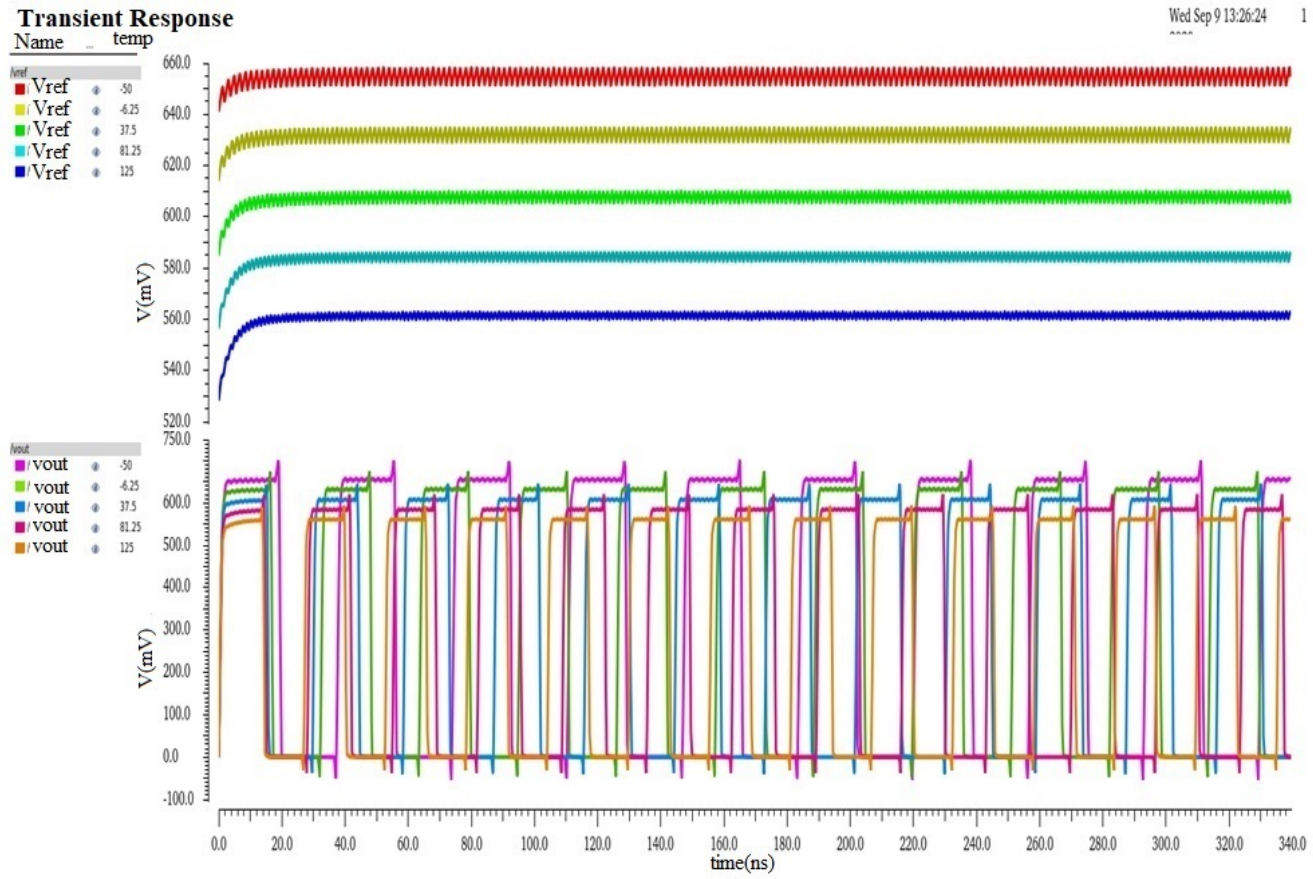

Figure 11. Simulation waveform of PVTCS with different temperature

TABLE III. Representation of Vref and Vout w.r.t. Temperature Variation

Temperature(^{0}C)	Vref(V)	Vout(V)
-50	1.34	1.49
0	1.46	1.53
50	1.57	1.61
100	1.62	1.65
130	1.71	1.68

A. *Process Corner Analysis*

The process corner analysis shows whether the design is accepted in all conditions after fabrication process. Table V represents corner analysis for the reference voltage with respect to temperature variation. The parameter defines a corner frequency of the circuit on the basis of nmos and pmos. In this parameter FF represent as fast and fast where FS represents fast and slow where SF represents as slow and fast and SS represent as slow and slow.

B. *Monte-Carlo Analysis*

Monte Carlo simulation allows to test the process variation and mismatches in the devices. This analysis is done for the power dissipation of the proposed compensated supply circuit topology. In this analysis, the number of samples is 2000 and mean value is 82.752µ and the standard deviation value is 22.595µ. This analysis describes in terms of 6σ method.

C. *Layout of proposed design*

The layout of the proposed reference circuit is represented in figure 13. The width of this circuit is 85.545m, length is 44.275m and it's surface area of the proposed reference circuit is 3,787.05m^2. Figure 14 illustrates the layout of LDO. The width of this circuit is 269.22 m, length is 110.665m and surface area is 2,793.23m^2. The layout of proposed Ring Oscillator Circuit is represented in figure 15. The width of this circuit is 176.01m, length is 25.44m and surface area is 4,477.69m^2. The layout of Full design is represented in figure 16. The width of this circuit is 283.355m, length is 140.81m and surface area is 39,899.22m^2. The full circuit has resistors and capacitors. The layout of the capacitors used in design are made with para-capacitance layers and resistors are made with the help of poly-resistance layer. Table VI illustrates the layout of surface area of the design.

TABLE IV. Comparison of PVT with respect to reported work

PARAMETER	TVLSI[5]	TVLSI[6]	TVLSI[12]	THIS WORK
YEAR	2011	2012	2014	2021
TECHNOLOGY(nm)	65	65	65	180
POWER(μW)	N/A	N/A	734	203
BODY BIAS	Yes	Yes	No	No
PROPORTIONAL VARIATION	82.1%	84.8%	45.2%	42.6%
TEMP VARIATION	N/A	N/A	91%	78.6%

TABLE V. Corner analysis for frequency(MHz)of PVTCS under Temperature Variation w.r.t. Proportional Analysis

Parameter	-50	-10	30	70	110	130
FF	48.6	43.5	39.9	34.8	31.0	29.21
FS	3.28	5.34	7.15	8.74	10.1	10.8
SF	10.6	6.20	2.28	1.09	4.10	5.483
SS	26.2	28.0	29.7	31.2	32.6	33.4

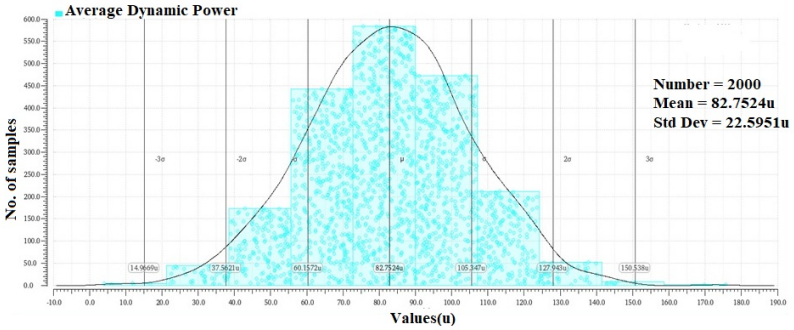

Figure 12. Monte-Carlo Analysis in terms of Power

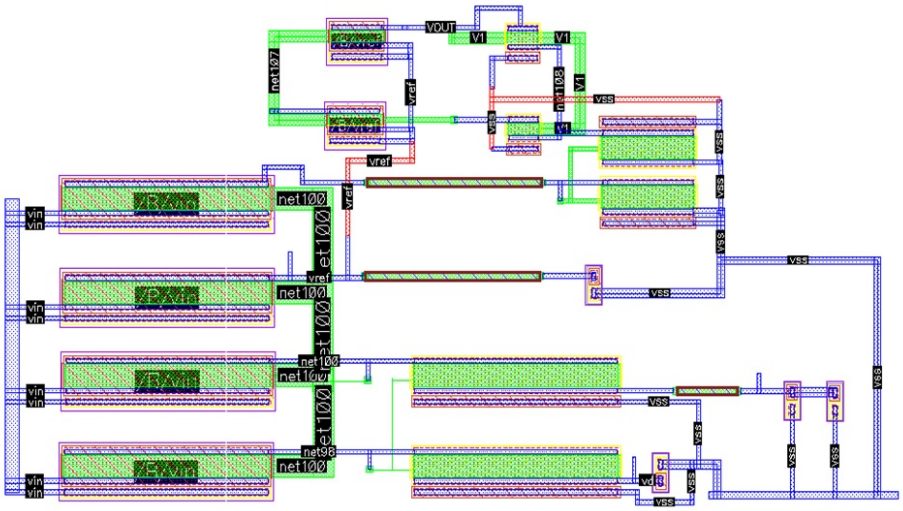

Figure 13. Layout of Proposed Reference Circuit

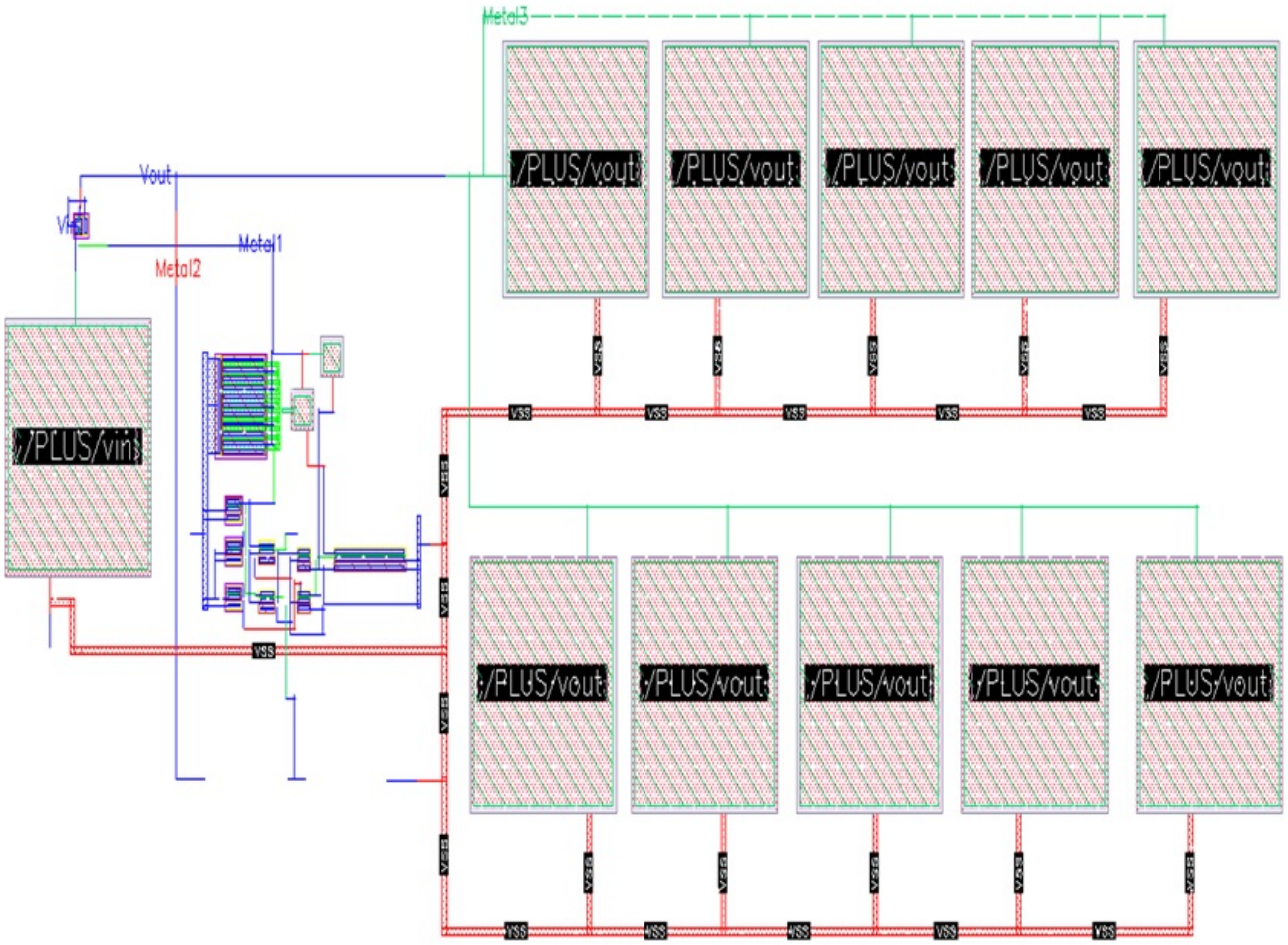

Figure 14. Layout of LDO Circuit

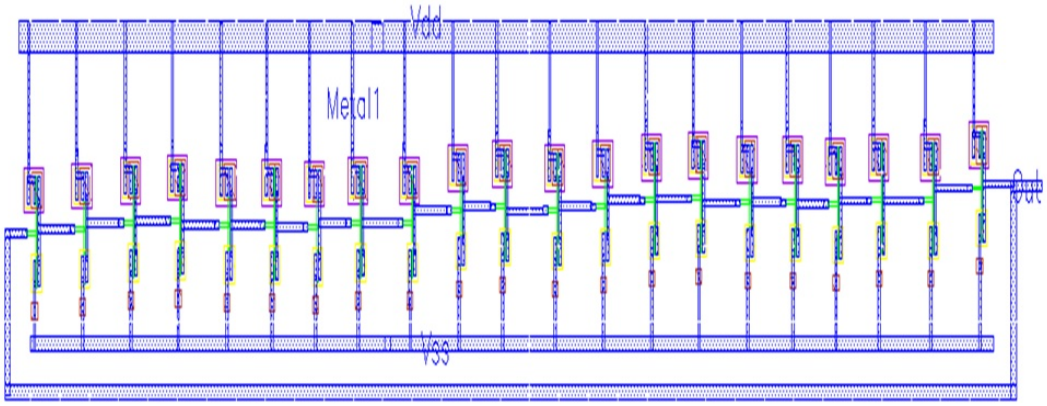

Figure 15. Layout of Ring Oscillator Circuit

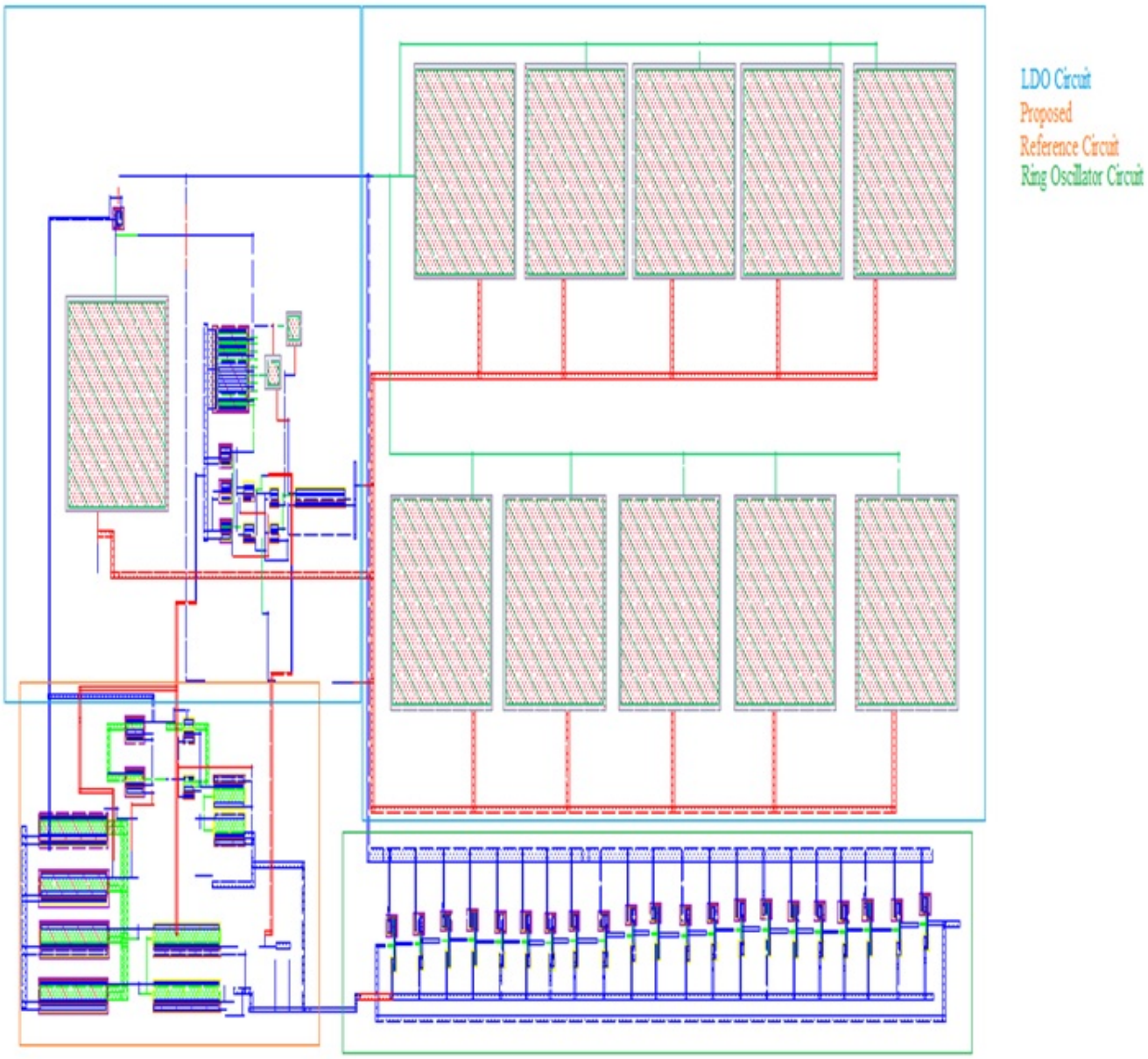

Figure 16. Layout of PVTCS circuit with ring oscillator

TABLE VI. Layout of Design

PARAMETER	Proposed Reference Circuit	LDO	Ring Oscillator	Full Circuit
Width(W)m	85.545	269.22	176.01	283.355
Length(L)m	44.275	110.665	25.44	140.81
Surface Area(A)m^2	3,787.05	2,793.23	4,477.69	39,899.22

5. CONCLUSION

There is a huge requirement for protection from supply variation and temperature variation in digital circuits, analog circuits, radio frequency circuits and many more. A PVTCS provides an approximate constant voltage to the load, so that a load does not directly affect from the supply variation. A proposed circuit provides constant voltage to the load with the help of CTAT and PTAT techniques. These techniques are implemented with the help of current mirror.All the simulations of the proposed design are done on the CADENCE software with 65nm technology. The low drop-out voltage regulator circuit is also designed for obtaining the constant voltage at load. A ring oscillator is used as a load. This oscillator contains twenty-one inverters with same (W/L) ratio to provide perfect oscillation without any supply disturbance. PVTCS based circuit has advantage in stability at the cost of surface area. PVTCS is responsible for improving the performance and stability of the circuit. The static power consumption is only 112.55 μW and dynamic power consumption is 91.09μW. In the proposed reference circuit, reference voltage provides 0.9±5mV that is sufficient for load of the circuit. Total input referred noise is 5.26×10^{-5} V/$\sqrt{Hz}$ and out frequency is 413.8MHz.

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