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Cell Optimization and Realization of Vedic Multiplier Desing in QCA

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Abstract: The construction of devices with smaller sizes, lower power dissipation, and higher speeds is a significant problem in contemporary computational technology. Technology advancement is required to get improved power dissipation, size, and speed optimization. By incorporating numerous architectural and behavioural alterations in the current technologies, researchers are attempting to identify ways and means. Designing digital circuits based on reversible logic and implementing them in quantum cellular automata is one such potential approach (QCA). The propagation delay in a multiplication operation is mostly caused by the addition of partial products and the production of partial products. This study proposes a Vedic multiplier based on UrdhwaTriyakbhyam. It has been found that the suggested designs of a Half Adder, 4-bit Ripple Carry Adder, 2×2 Vedic Multiplier, followed by 4×4 Vedic Multiplier and 8×8 Vedic Multiplier circuits have resulted in reductions of 68.75%, 72.64%, 44.84%, 43.44%, and 60.00% in the circuit size, respectively. When compared to previously proposed circuits, improvements in the area have also been observed, with increases of 57.14%, 55.55%, 48.45%, 28.03%, and 42.57% in the area of the Half Adder Circuit, 2×2 Vedic Multiplier, 4-bit Ripple Carry Adder, 4×4 Vedic Multiplier, and 8×8 Vedic Multiplier circuits, respectively. Numerous parameters like area, clock latency, and quantum cost were calculated using the QCAD tool.

Keywords: Quantum dot cellular automata(QCA), CMOS, Half Adder, Ripple Carry Adder, Vedic Multipliers

1. INTRODUCTION

A non-transistor estimation technique called quantum-dot cellular automata (QCA) encrypts binary data by setting up charges between quantum dots. Despite the fact that traditional CMOS has been the dominant technology in the manufacturing industry for several decades. We presently live in a more technologically advanced period, therefore our requirement for Low power, a smaller area, and higher speed cannot be fulfilled using CMOS technology as is standard[1][2]. The improvement in the cell count is used as an advantage to propose Vedic multipliers(VM) with optimized architecture and a reduction in function cost. QCA-based architectures are best while incorporating more or less obvious advantages such as steadiness, quickness, minimal space, and less energy usage[3][4].Researchers have also considered nano computing to increase the QCA's number of arithmetic operations, and various designs have been created. Since multipliers are a fundamental part of the majority of computerized frameworks, including Digital Signal Processing, etc[5]. Many unutilized concepts for sophisticated binary multipliers have been outlined due to the advancement of innovation. The optimization of cells was the central focus of this article and implementation of the various types of QCA multiplier, which was accomplished by using effective and simpler Ripple Carry Adder (RCA) and QCA half adder(HA) circuits[6][7]. A crucial element that shines in regards to latency, quantum cost, and area are the proposed multipliers. The QCA simulation environment has been used to extensively evaluate the earlier array multiplier[8][9]. However, there are also extremely rapid and low-hardware-architecture-required arithmetic functions that use the Vedic methodology[10]. This will be used to improve how quickly all CPUs compute. For achieving partial product summing in larger order multipliers, a considerable quantity of adders is employed. One approach that utilizes the 16 Vedic Sutrasis the Vedic Multiplier system, explains how to solve all mathematical problems quickly and easily[11][12][13].

A. Paper Organization:

The study is summed up by stating that Section 1 tells us about basic introduction to QCA, and Section 2 defined the QCA terminologies. In section 3,newly proposed QCA-based layouts have been included. The designs are presented in such a way that each of them can act as a stepping stone in designing more complex circuit. Firstly, 1-bit Half Adder has been designed which is further used to proposed to design an optimized 2×2 Vedic Multiplier circuit. On the other hand, a previously designed 1-bit Full Adder is used to design newly proposed and highly optimized 4-bit Ripple

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Carry Adder. Now with the help of 4-bit RCA and 2×2 VM a newly proposed 4×4 QCA based VM is designed. Lastly, using 8-bit RCA (obtained by cascading two 4-bit RCA) and 4×4 VM a newly proposed 8×8 VM is designed. Therefore, it can be concluded that each proposed design is further used in designing of more complex circuit. Section 4 displays the output waveform of the proposed circuits and their comparison with previously proposed circuits. Calculation of energy dissipation parameters of suggested architectures as well as performance comparison in terms of cell count, total area occupied, clock latency and quantum cost has also been included in this manuscript.

2. TERMINOLOGY FOR QUANTUM DOT CELLULAR AUTOMATA:

Quantum cell action is arranged in a QCA. Information from nearby cells is electrostatically propagated by the cell. Twin electrons are elaborated in a cubical-shaped cell[14]. When the input cell in QCA is excited then some amount of energy is released and at the same time the information is passed to the succeeding cell therefore we can say that cell-to-cell interaction produced by electron position rearrangement provides QCA cell connectivity[15][16]. In Quantum-dots of a QCA cell, electron pairs are stuffed in antipodal sides. The electronic sites, known as "Quantum Dots," represent the locations where electrons can exist. Tunnel junctions connect dots. The lines connecting the Quantum dots represent tunnelling paths.We can see that figure 1(a) is a functional diagram of a QCA cell (a) and figure 1(b) and 1(c) 1 represent the polarization levels that equate to Boolean logics zero and one[17].

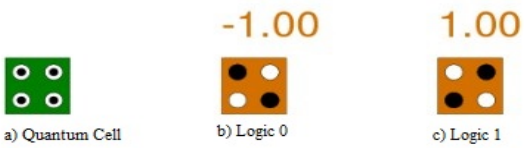

Figure 1. (a)Basic Quantum Cell,(b)Logic'0',(c)Logic'1'

A. *Majority Gate Logic:*

There are total 5 cells in the majority gate circuit (having three inputs). The majority logic gate's block diagram is shown in Fig.2. It consists of 3 cells acting as input-bits, one QCA cell in the middle, and one cell acting asoutput[18][19]. The Three-I/P majority gate offers the flexibility to implement basic AND or OR logic operations by designating one of the input cells as the control input. By assigning a logic 1 or logic 0 value to the control input, the gate can be configured accordingly.Moreover, by placing a QCA cell at an angle of 45º at the output of AND and OR gates we can obtain NAND and NOR logic. Therefore, The 3-Input majority gate serves as the fundamentalcomponent of any QCA-based circuit, acting as the essential building block[20][21].

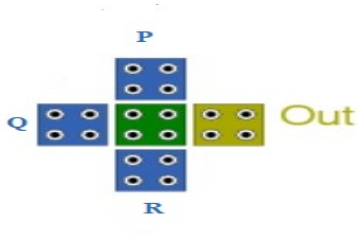

Figure 2. 3-Input Majority Gate

B. *Clocking scheme in QCA:*

The clock plays the most crucial role in transferring information. There is a total of four clock zones namely: clock zone 0 or switch phase, in this the potential energy barrier is raised and the cells start polarizing, clock zone 1 or hold phase, in this phase the previously polarized cells are used to excite the succeeding cells in the queue, clock zone 2 or release phase in this phase the potential barrier starts disappearing and as a result, the cells start depolarizing, clock zone 3 or relax phase in this phase the cells are unpolarized[22][23]. Each clock is lagging behind by 90 degrees from the succeeding clock. The clocking scheme in QCA is shown in fig.3 in which clock zone are represented with different colors, the input cell is marked with yellow color and the output cell is marked with blue color[24][25].

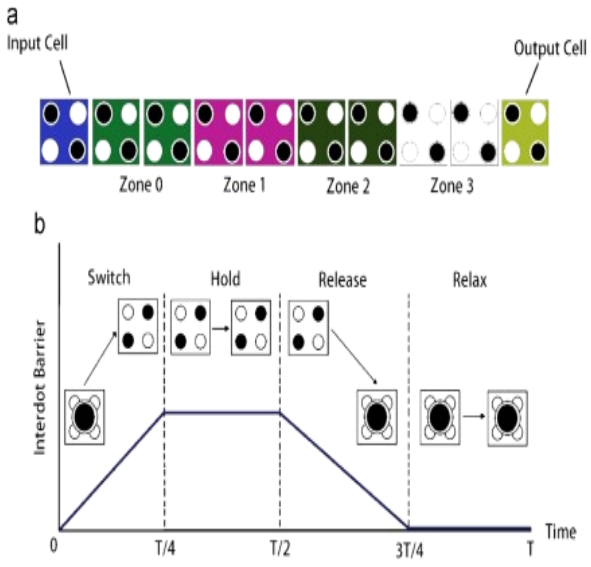

Figure 3. Clocking scheme in QCA

3. LOGIC CIRCUIT ARCHITECTURES PROPOSED USING QCA:

In this section, we'll discuss newly proposed designs of a Half Adder, 2×2 VM, 4-bit RCA, 4×4 VM and 8×8 VM and will also investigate why these proposed designs are superior than their previous counterparts.

A. *Proposed Half Adder:*

Modern ICs and ALUs in electronics that carry out binary number accumulation are built on adders. The newly proposed design of QCA-based HalfAdder is represented by fig.4. The proposed QCA HA is made with the help of 2-Input XOR gate[26]. The sole purpose of designing half adder circuit is that, it can further be used to design 2×2 Vedic Multiplier. Assuming A and B are two input values, the formula represented with equations 1 and 2 can be used to estimate Sum and carry.

Sum= AB .....(1)

Carry= AB.....(2)

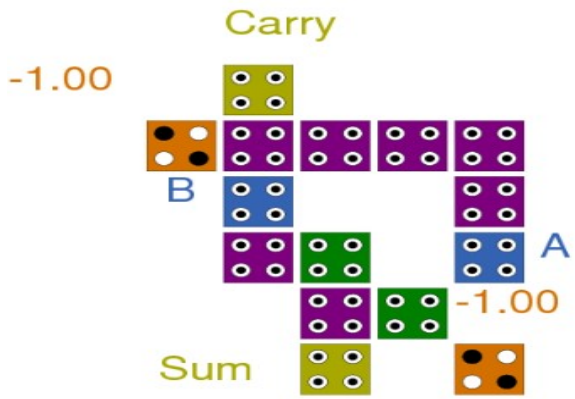

Figure 4. QCA Layout of Half Adder **(N15)**

B. *Proposed 2×2 VM:*

The Urdhva-Tiryakbhyam-based Vedic Multiplier was created for both binary and decimal multiplication. A Vedic multiplication can be used for bitwise multiplication, products, and column-wise additions. The primary function of Vedic multiplier is their capability to simultaneously compute partial products and perform summation. This characteristic is particularly common in Vedic multipliers. The process involved in multiplying 2×2 bits can be easily explained.

1. An AND gate will be used to multiply A0 and B0 first. The core task involves the cross-multiplication of A and B, which necessitates the utilization of two AND gates. This process generates the output S0, represented as S0 =A0B0.
2. A multiplication operation is performed between A's LSB and B's MSB. The products of these operations are then added together by a half adder to produce the output C1S1.
3. The prior carry C1 is added using the second HA, and the final product, C2S2, is equal to C1 plus A1B1. Multiply the MSB of A and the MSB of B, or (A1B1).
4. The output namely C2S2S1S0 is then produced after multiplying two binary integers by two.

The conventional block architecture of 2×2 VM is represented by figure 5 and the proposed QCA layout of 2×2 VM is shown in figure 6 which has a total cell count of 107 and an occupied area is 0.024 μm^2*having an overall delay of 0.25 units.*

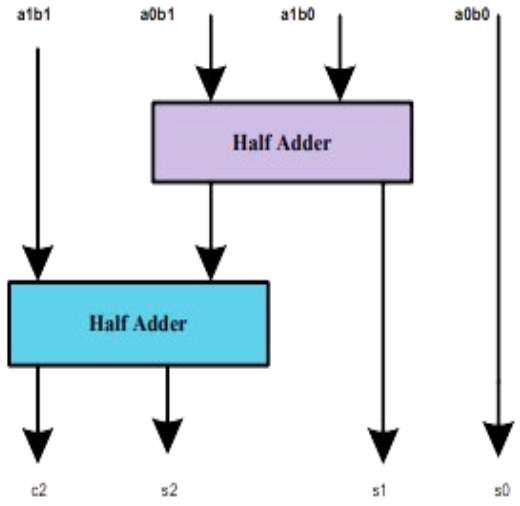

Figure 5. Block Architecture of 2×2 Vedic Multiplier

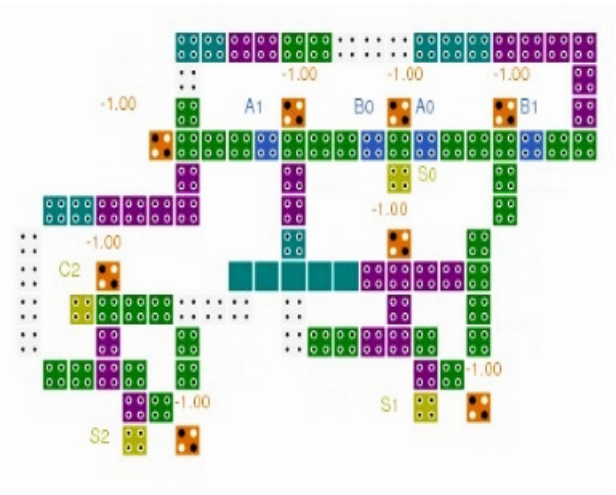

Figure 6. Proposed 2×2 VM QCA layout **(N107)**

C. *Proposed 4-bit RCA:*

The summation of an n-bit binary sequence is accomplished by connecting a series of n full adders in a cascading structure. In an RCA (Ripple Carry Adder) circuit, each individual adder stage generates a carry output because it is constructed using cascaded full adders. The carry outputs generated at each full adder stage are forwarded to the subsequent full adder stage, where they serve as carry inputs. This sequential process persists until the final full adder stage is reached. In a complete adder circuit, each carry output bit is successively propagated to the subsequent stage. This characteristic is the reason why it is referred to as a "Ripple Carry Adder," as depicted in figure 7.

The crucial feature of a carry adder is its capability to add input bit sequences of varying lengths, such as 4 or

5 bits. However, it's important to note that the final output of theadder is determined only after the carry outputs from each adder stage have been computed and propagated to the next stage. Consequently, using this carry adder introduces a delay in obtaining the final result. The proposed 4-bit RCA is depicted in the diagram fig8. Four full adders are connected in back-to-back fashion which forms a cascade-like structure. The carry input bit (Cin) is always zero. When this initial carry 'Cin' is applied to the 2 input bits namely A1 A2 A3 A4 and B1 B2 B3 B4. then it produces output represented with S1 S2 S3 S4 and C4(Final carry).

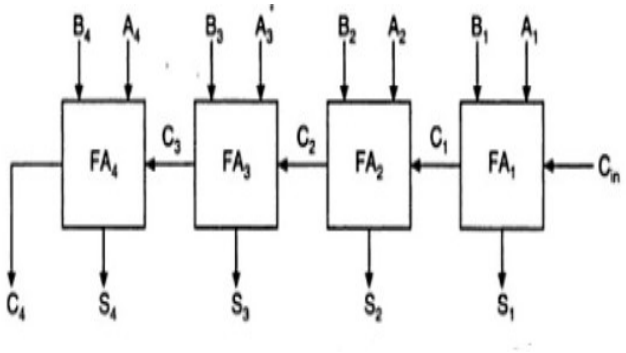

Figure 7. Block Diagram Architecture of 4-bit RCA

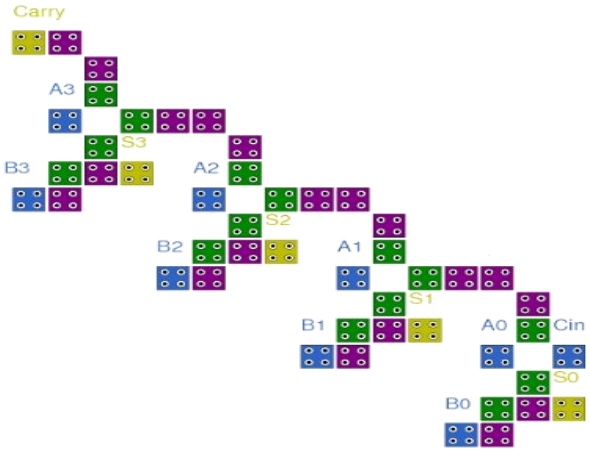

Figure 8. QCA-based Proposed 4-bit RCA **(N48)**

D. Proposed 4×4 Vedic Multiplier:

Using a cascade connection, a 4-bit Ripple Carry Adder (RCA) was constructed by utilizing multiple instances of a 1-bit Full Adder circuit. As shown in fig.9, the 4x4 VM circuit is executed by utilizing four 2x2 VM circuits. To analyze the 4x4 multiplications, the bit sequences A and B can be divided into two equal parts. Let's use thenotations A3A2 and A1A0 for the two parts of A, and B3B2 and B1B0 for the two parts of B[15]. As seen in fig. 9, we can use the following structure for multiplication by employing the fundamentals of Vedic multiplication, which involves taking two bits at a time and using a 2-bit multiplier block. A suggested QCA 4-bit RCA with a 2-bit VM is included in the 4×4 VM. Newly designed 4-bit VM design is shown in Fig.10.

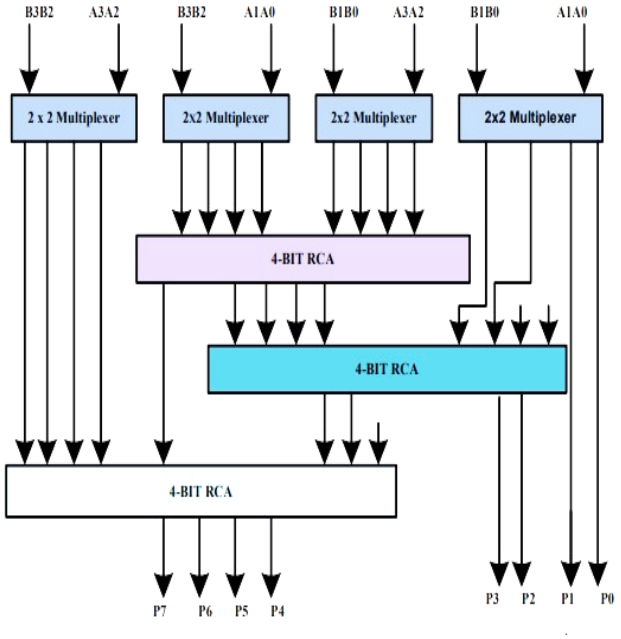

Figure 9. Block Architecture of 4x4 VM **(N1108)**

Figure 10. Proposed 4x4 VM **(N1108)**

E. Proposed 8×8 VM:

A total of four (4) 4×4 VM and 3(three) 8-bit RCA make up the 8-bit multiplier. The disadvantage of RCA is that it

must hold for the earlier carry in order to create the output. There are four recommended 4×4 VM in the proposed 8×8 VM. The conventional block diagram of 8×8 VM is shown in Fig.11.

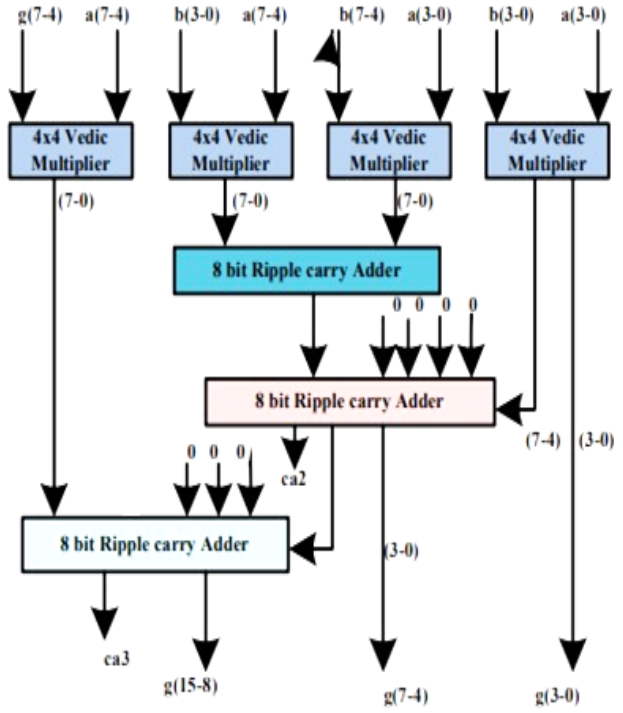

Figure 11. Block Architecture of 8×8 VM

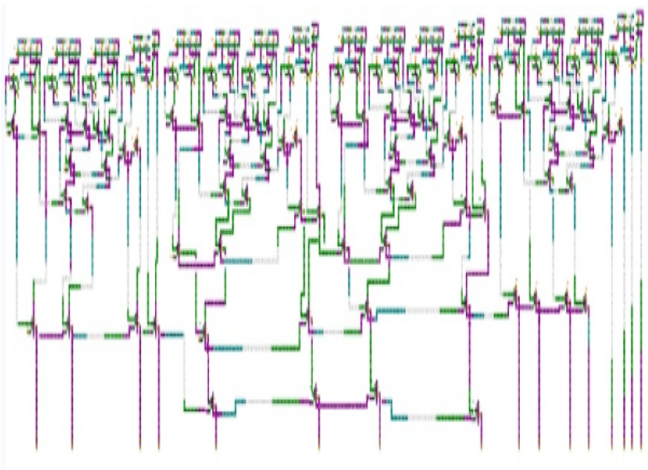

Figure 12. Proposed 8×8 VM **N7514**

A newly proposed QCA-based 8×8 VM circuit is represented by fig.12. This circuit is designed with the help of two four 4×4 VM and three 8-bit RCA. After performing its simulation, it is found that the proposed multilayer design has a total cell count of 7514 cells and an occupied area is 10.59 $\mu m^2 having an overall delay of 0.25 units$.

F. Proposed Conventional Formula for nn Vedic Multiplier Architecture:

The proposed fundamental structure of n-bit Vedic Multipliers is derived from the designed 8x8 Vedic Multiplier. The n-bit Vedic Multiplier comprises a combination of n/2 individual multipliers (four numbers), an n-bit Ripple Carry Adder (RCA) (one number), an n-bit Full Adder (FA) (one number), and an (n/2 - 1) bit Ripple Carry Adder (RCA) (one number).

Likewise, to execute the multiplication of a 16x16 Vedic Multiplier using a conventional formula, the architecture involves utilizing four 8x8 multipliers, a 16-bit Ripple Carry Adder (RCA) (one number), a 16-bit Full Adder (FA) (one number), and a 7-bit Ripple Carry Adder(RCA) (one number). The different components within the multiplier employ a traditional formula to determine parameters such as the count of majority gates and inverters used [24].In the 4x4 Vedic multiplier, there are seven full adders, nine half adders, and sixteen ANDgates. Each adder consists of two majority gates and one inverter.

The traditional method of computing the Majority Gate (MG) involves using the following formula: The 4×4 Vedic Multiplier contains a specific number of Majority Gates, which are used to calculate the absolute value. Maj.(4×4) = [(7FA×2) + (9HA×2) + (16 AND×1)] = 48 MG The absolute count of Majority Gates (MG) in the 8-bit Vedic Multiplier is determined through calculation.

Maj(8×8)= [4 × (Absolute count of Maj in 4×4 multiplier)] + [(8-bit FA + 8-bit RCA +3-bit HA) × 3] =[4×48] +[19×3] =249

Now, the computation of the absolute count of Majority Gates (MG) in an n-bit Vedic Multiplier is performed.

Maj.(n×n) = [4 × (Absolute count of Maj.in n/2 × n/2)] + [3 × (n + n + n 2 - 1)] = [4 × (Maj.n/2 × n/2)] + [3× (5n 2 1)]..... (3)

Conventional formula for Inverter Calculation: The absolute count of inverters in the 4-bit Vedic Multiplier is being calculated as. Inv.(4×4) = [total no.of FA × 1] + [total no.of HA × 1] =[7×1] + [9×1]=16.

The absolute count of inverter counts in the 8-bit Vedic Multiplier is being determined through calculation.

Inv.(8×8) = [4 × (Inv.(4 × 4))] + [(8FA + 8RCA + 3HA) × 1] =[4×16] +[19×1] = 83

Now, the calculation of the absolute count of inverter count in n-bit Vedic Multiplier is

Inv.(n×n) =[4 × Inv.(n 2 × n 2)] +(5n 2 - 1).....(4)

Based on the formulation and conventional expression described above, the proposed structure of the n-bit Vedic Multiplier is depicted in Figure13.

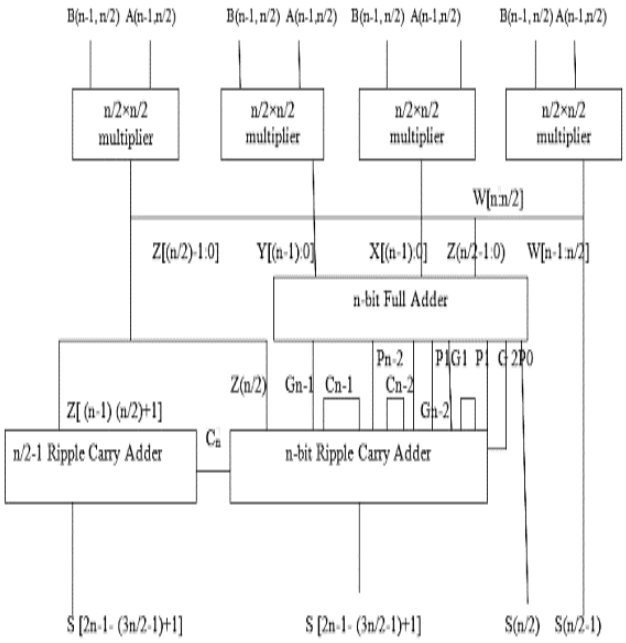

Figure 13. The conventional structure of the n-bit Vedic Multiplier

4. SIMULATION RESULT AND DISCUSSION:

QCADesigner is a widely recognized tool that is commonly employed for estimating QCA (Quantum-dotCellular Automata) circuits. Figures 14,15,16,17,18 successively illustrate the resultant output waveforms of the proposed Half Adder, 2×2 VM, 4-bit RCA, 4×4 VM, and 8×8 VM, demonstrating the effectiveness of the suggested circuits.

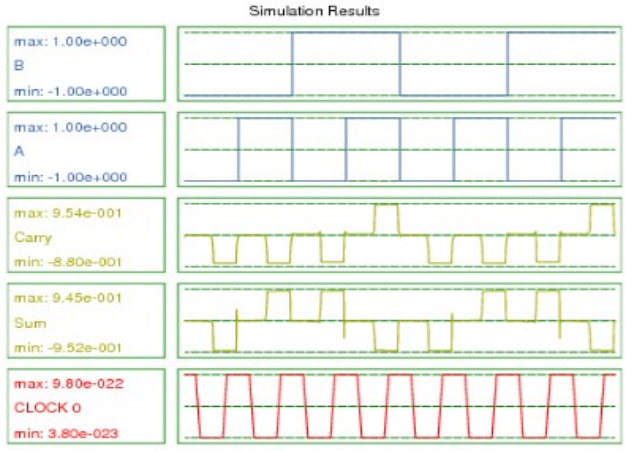

Figure 14. Waveform of HA Circuit (N15)

Comparison of newly proposed designs of 1-bit half adder, 2x2, 4x4 and 8x8 Vedic Multiplier with their previous counterparts is shown in table I,II,III,IV,V respectively. Based on the data presented in the table, it can be concluded

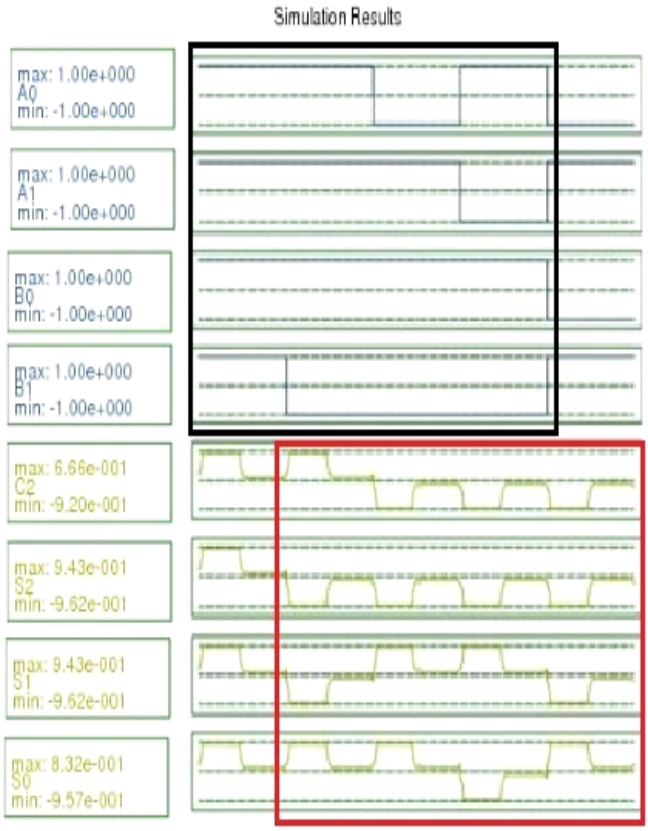

Figure 15. Waveform of 2×2 VM **(N107)**

that the proposed designs exhibit high-optimization and superiority in terms of cell count, area,clock latency, and quantum cost.

To substantiate the optimization of the proposed designs, several key factors can be considered: Cell count: Comparing the cell count of the proposed designs with alternative designs or existing benchmarkscan demonstrate if the proposed designs effectively reduce the number of cells required for a given functionality.
Area: Analyzing the area requirements of the proposed designs in comparison to other designs can indicatewhether they achieve a more compact layout, resulting inreduced space utilization.
Clock latency: Evaluating the clock latency of the proposed designs in relation to similar designs canhighlight whether they achieve faster operation or reduced delay in obtaining the output.
Quantum cost: Assessing the quantum cost of the proposed designs compared to alternative approaches can determineif they provide a more efficient utilization of quantumresources.
Trend for reduction in the number of cell count is shown in represented by figures 192021 respectively where the Y-axis represents the cell count and X-axis shows comparison

TABLE I. PERFORMANCE COMPARISON OF 1-BIT HA

HA Designs	Cell Count	Area(μm^2)	Clock Latency	Quantum Cost
[1]	48	0.370	0.50	0.185
[2]	48	0.056	0.75	0.042
[3]	39	0.040	075	0.030
[4]	16	0.028	0.50	0.007
N15	**15**	**0.024**	**0.25**	**0.006**

TABLE II. PERFORMANCE COMPARISON OF 2x2 VM

2X2 VM	Cell Count	Area(μm^2)	Clock Latency	Quantum Cost
[11]	194	0.270	2.25	0.671
[3]	194	0.270	1.75	0.473
[12]	135	0.190	2.00	0.380
[13]	121	0.170	2.00	0.340
[14]	119	0.150	2.00	0.300
[4]	115	0.130	1.00	0.130
N107	**107**	**0.120**	**0.50**	**0.060**

TABLE III. PERFORMANCE COMPARISON OF 4-BIT RCA

4-BIT RCA	Cell Count	Area(μm^2)	Clock Latency	Quantum Cost
[6]	212	0.194	0.50	0.097
[7]	209	0.301	1.25	0.376
[8]	125	0.189	0.50	0.095
[9]	70	0.170	0.75	0.127
N48	**48**	**0.108**	**0.75**	**0.075**

TABLE IV. PERFORMANCE COMPARISON OF 4x4 VM

4x4 VM	Cell Count	Area(μm^2)	Clock Latency	Quantum Cost
[10]	1959	2.390	1.50	3.581
[15]	1955	2.250	4.25	9.563
[3]	1726	2.040	5.25	10.710
[14]	1234	2.350	1.25	2.937
N1108	**1108**	**1.720**	**0.75**	**1.290**

between previous and our proposed designs. Initially, to design a basic 2x2 VM 194 cells [11] but our proposed design uses only 107 cells (as shown in fig.19) thereby resulting in 44.84% reduction in the cell count. We can also see that for designing 4x4 VM initially 1959 cells [10] are required but our proposed design uses only 1108 cells (as shown in fig. 20) to get the desired output thereby resulting in 43.44% reduction in the cell count. Similarly, to design 8x8 VM initially 26,973 cells [26] are required but our proposed design uses only 7,154 cells (as shown in fig 21), resulting in 73.47% reduction in the cell count.

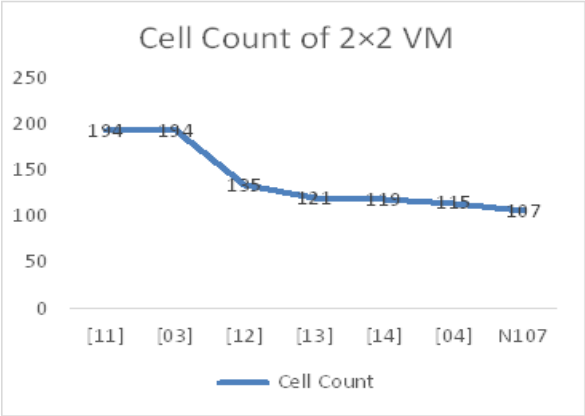

Figure 19. Trend for 2x2 VM

TABLE V. PERFORMANCE COMPARISON OF 8x8 VM

8x8 VM	Cell Count	Area(μm^2)	Clock Latency	Quantum Cost
[10]	26,499	82.190	38.00	3123.220
[15]	15,106	22.570	30.00	677.100
[3]	13,839	21.490	30.00	644.700
[14]	13,533	18.440	10.15	194.910
N7514	**7514**	**10.590**	**1.75**	**18.530**

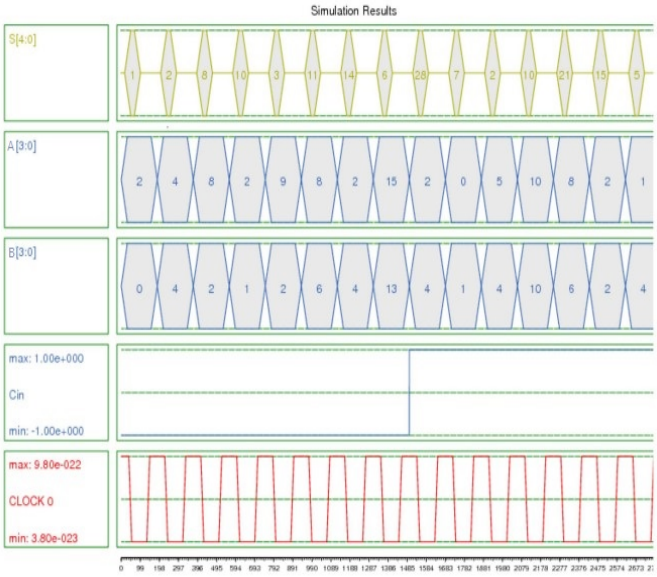

Figure 16. Waveform for 4-bit RCA (N48)

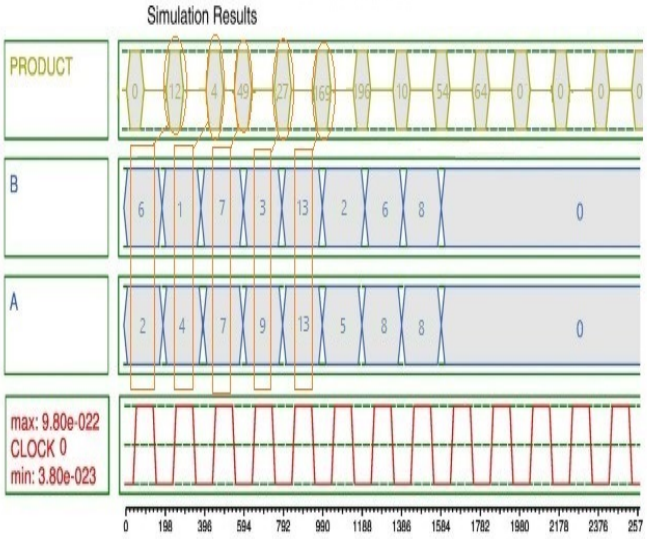

Figure 17. Waveform for 4X4 VM

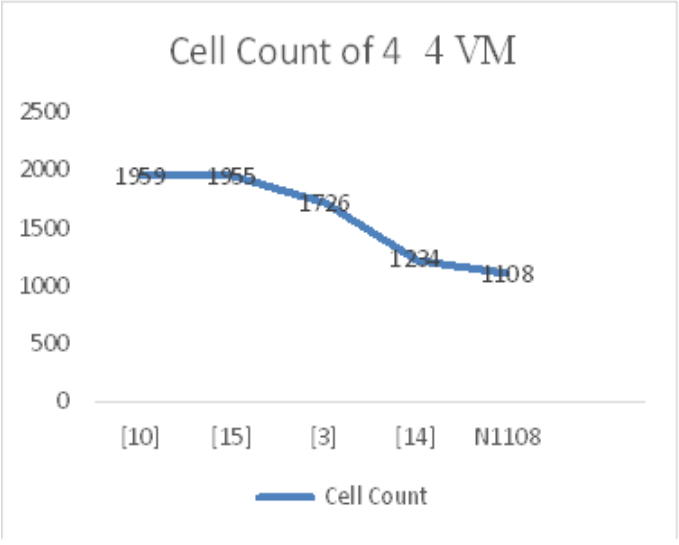

Figure 20. Trend for 4×4 VM

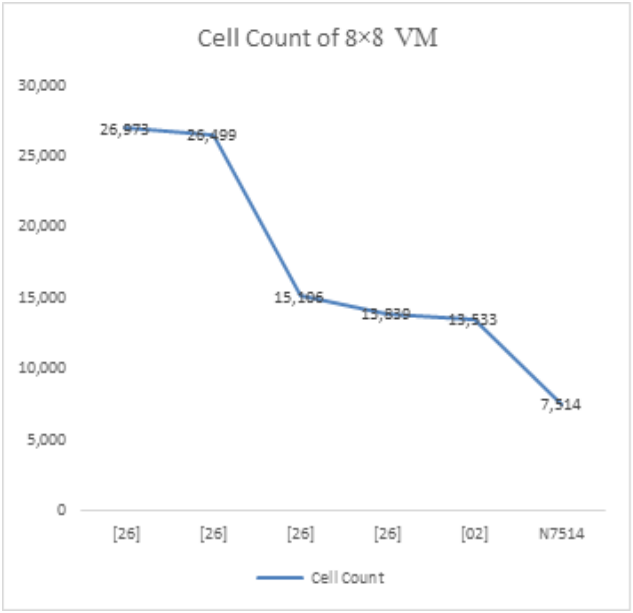

Figure 21. Trend for 8-bit Multipliers

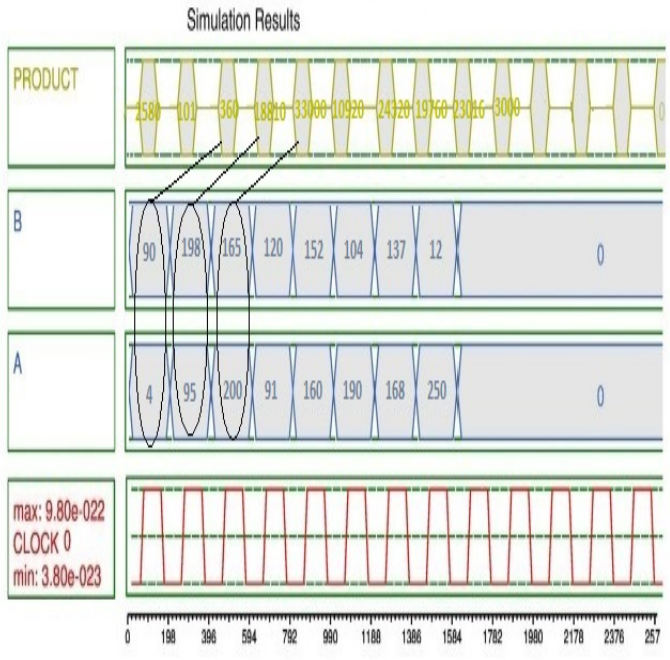

Figure 18. Waveform for 8X8 VM

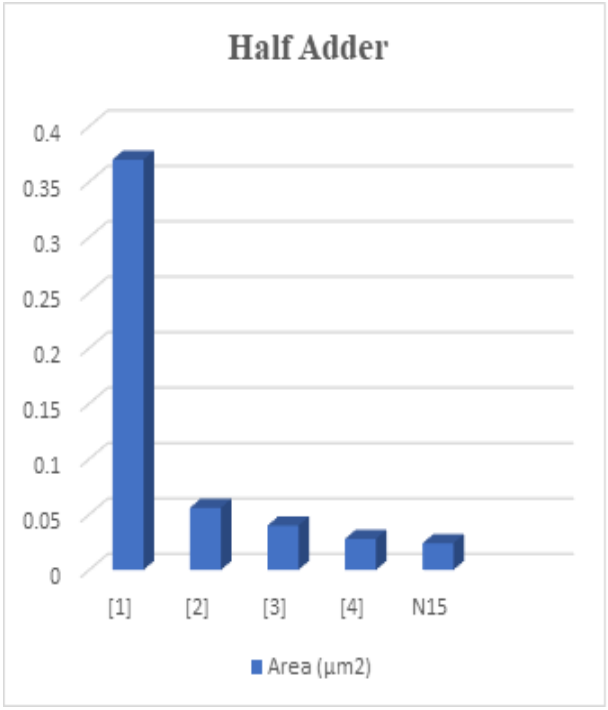

Figure 22. For HA

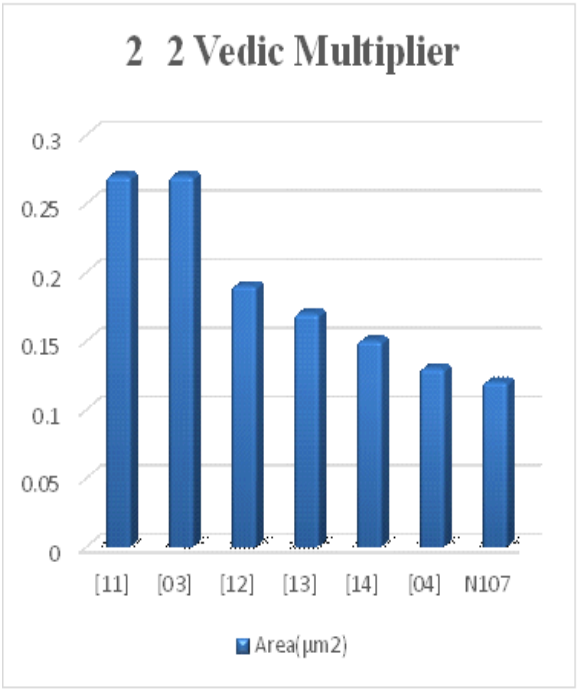

Figure 23. For 2×2 VM

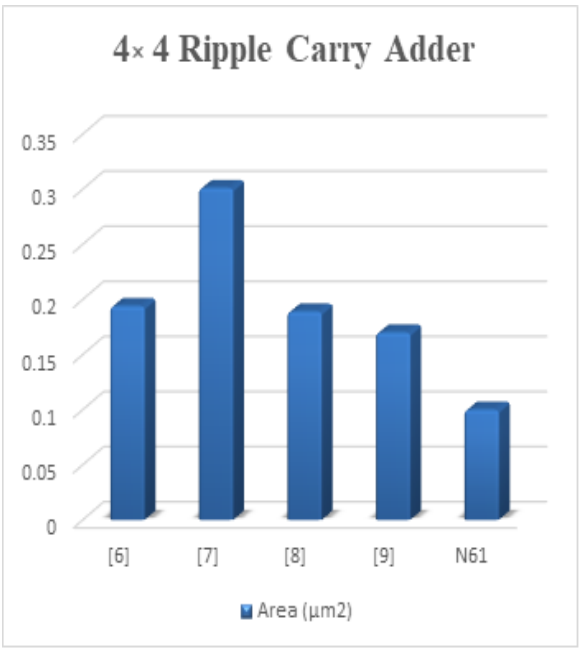

Figure 24. For 4-bit RCA

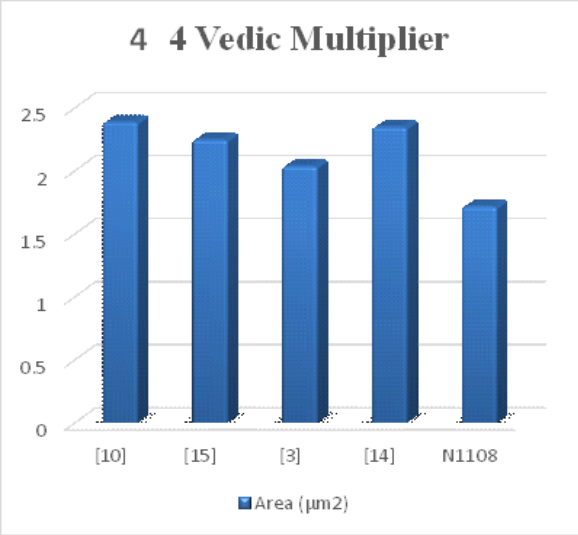

Figure 25. For 4×4 VM

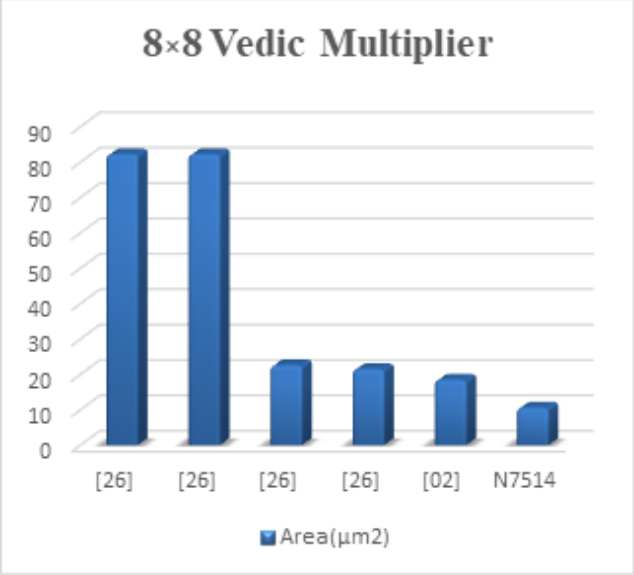

Figure 26. For 8-bit Multiplier

Comparison of the area of various QCA based adders and multipliers is shown in figure 22, 23 24, 25 26 for half adder, 4-bit RCA, 2×2 VM, 4×4 VM and 8×8 VM respectively. From the figures, we can clearly see that our proposed designs occupies very less area as compared to previously proposed designs and hence we can say that our proposed design is highly efficient.

A. *Energy Dissipation Analysis of Proposed Desings:*

Using the recently developed tool QCA DesignerE and treating each QCA coordinate as an energy ”bath,” energy dissipation is carried out. Since, at the beginning of the clock cycle, the QCA cell is in a depolarized state; energy from the clock must be received and encircled by cells in order to attain a polarization state.

The cell enters the depolarized state by reviving the clock and distributing energy to the enclosing cells at the end of the clock cycle. Here, some energy is also lost to the surrounding area. Energy dissipation calculation at 1K temperature for HA circuit, 2×2 VM, 4-bit RCA, 4×4 VM and 8×8 VM is shown in tables VI VII VIII IX X respectively.

The parameters Ebtx is the total amount of energy used by all cells, calculated for each clock cycle.

Ectx the total amount of energy that is transferred between cells for each clock cycle. EEtx represents the number of total errors in the cell's energy estimation. Sb stands for reflects the total amount of energy released by the cells. Ab indicates the standard error for each clock cycle and the average criteria for energy transfers to the bath.

While Ac illustrates how energy typically moves through a clock cycle, Sc is the average energy flow to or from the clock throughout the course of the simulation. For entire simulation procedure and calculation of energy we select bistabel mode for best results as can been seen in fig27

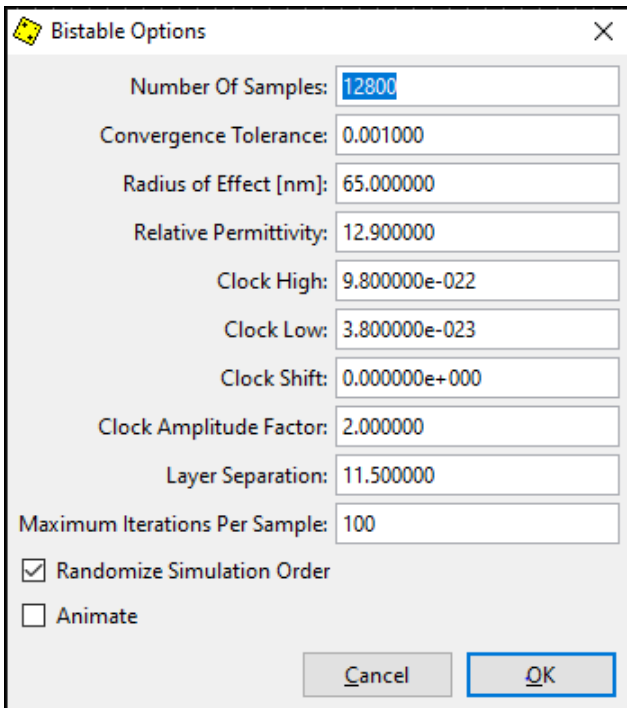

Figure 27. Bistable simulation Mode

5. Conclusions and Future Work

A nano architectural computation technique called QCA is used to create digital circuits. The semiconductor sector

TABLE VI. ENERGY DISSIPATION OF 1-BIT HA

$E_{btx}(eV)$	$E_{ctx}(eV)$	$E_{Etx}(eV)$	$S_b(eV)$	$A_b(eV)$	$S_c(eV)$	$A_c(eV)$
6.34 e$^-$004	2.96 e$^-$004	-6.30 e$^-$005				
6.26 e$^-$004	1.32 e$^-$003	-6.36 e$^-$005				
1.16 e$^-$003	9.78 e$^-$004	-1.24 e$^-$004				
1.23 e$^-$003	5.31 e$^-$004	-1.29 e$^-$004				
6.33 e$^-$004	2.96 e$^-$004	-6.30 e$^-$005	9.73 e$^-$003	8.85 e$^-$004	8.85 e$^-$005	8.00 e$^-$004
6.26 e$^-$004	1.30 e$^-$003	-6.36 e$^-$005	Er: -1.10 e$^-$003	Er: -9.19 e$^-$005		
1.17 e$^-$003	9.70 e$^-$004	-1.24 e$^-$004				
1.22 e$^-$003	5.30 e$^-$004	-1.29 e$^-$004				
6.33 e$^-$004	2.90 e$^-$004	-6.30 e$^-$005				
6.26 e$^-$004	1.30 e$^-$003	-6.36 e$^-$005				
1.17 e$^-$003	9.70 e$^-$004	-1.24 e$^-$004				

TABLE VII. ENERGY DISSIPATION OF 2x2 VM

$E_{btx}(eV)$	$E_{ctx}(eV)$	$E_{Etx}(eV)$	$S_b(eV)$	$A_b(eV)$	$S_c(eV)$	$A_c(eV)$
2.24 e$^-$003	3.10 e$^-$003	-1.80 e$^-$004				
2.73 e$^-$003	6.52 e$^-$004	-2.28 e$^-$004				
2.85 e$^-$003	5.07 e$^-$004	-1.16 e$^-$004				
5.27 e$^-$003	-1.11 e$^-$004	-5.14 e$^-$004				
2.59 e$^-$003	1.20 e$^-$003	-2.17 e$^-$004				
2.45 e$^-$003	1.60 e$^-$003	-2.15 e$^-$004	3.62 e$^-$003	8.85 e$^-$004	8.81 e$^-$003	8.00 e$^-$004
1.54 e$^-$003	1.60 e$^-$003	-3.82 e$^-$004	Er: -3.23 e$^-$003	Er: -2.94 e$^-$004		
4.21 e$^-$003	1.22 e$^-$004	-5.53 e$^-$004				
2.42 e$^-$003	1.42 e$^-$003	-1.82 e$^-$004				
2.79 e$^-$003	4.66 e$^-$004	-2.41 e$^-$004				
3.13 e$^-$003	9.01 e$^-$004	-2.75 e$^-$004				

TABLE VIII. ENERGY DISSIPATION OF 4-BIT RCA

$E_{btx}(eV)$	$E_{ctx}(eV)$	$E_{Etx}(eV)$	$S_b(eV)$	$A_b(eV)$	$S_c(eV)$	$A_c(eV)$
1.02 e$^-$003	1.84 e$^-$003	-9.91 e$^-$005				
1.52 e$^-$003	1.17 e$^-$003	-1.47 e$^-$004				
1.53 e$^-$003	1.18 e$^-$003	-1.53 e$^-$004				
1.36 e$^-$003	1.91 e$^-$003	-1.32 e$^-$004				
1.05 e$^-$003	2.13 e$^-$003	-9.65 e$^-$005	1.67 e$^-$002	1.52 e$^-$003	6.34 e$^-$003	5.77 e$^-$004
1.71 e$^-$003	9.64 e$^-$004	-1.74 e$^-$004	Er: -1.65 e$^-$003	Er: -1.50 e$^-$004		
1.73 e$^-$003	9.22 e$^-$004	-1.70 e$^-$004				
1.36 e$^-$003	1.59 e$^-$003	-1.36 e$^-$004				
1.46 e$^-$003	1.48 e$^-$003	-1.47 e$^-$004				
1.94 e$^-$003	8.49 e$^-$004	-1.94 e$^-$004				
1.94 e$^-$003	8.59 e$^-$004	-1.99 e$^-$004				

has improved over Modern standard CMOS technology and has shown to be a better alternative to earlier automation techniques. A few revolutionary technologies include quantum computing, molecular computing, and highly effective nanotechnology. Coulomb's repulsion-based nanotechnologies are in use. This paper provided the best method for putting all suggested circuits into action.

At the nanoscale level, QCA proves to be a credible and dependable alternative to CMOS technology. QCA is an acceptable and trustworthy substitute for CMOS technology scalability in terms of faster, more efficient, and denser technology.

The suggested designs have additionally reduced the cell count which eventually led to reduction in the overall area occupied by the desings. In this manuscript, we have proposed a novel HA Circuit, 2×2 VM, 4-bit RCA, 4×4 VM and 8×8 VM with a reduced number of cells resulting in lesser occupied as compared to the previously proposed design thereby resulting in 68.75%, 44.84%, 72.65%, 43.44% and 44.45% reduction in the size of the circuits respectively.

TABLE IX. ENERGY DISSIPATION OF 4x4 VM

$E_{btx}(eV)$	$E_{ctx}(eV)$	$E_{Etx}(eV)$	$S_b(eV)$	$A_b(eV)$	$S_c(eV)$	$A_c(eV)$
2.94 e$^-$002	-1.18 e$^-$002	-2.42 e$^-$003				
3.11 e$^-$002	1.65 e$^-$002	-2.60 e$^-$003				
3.01 e$^-$002	-1.44 e$^-$002	-2.49 e$^-$003				
3.28 e$^-$002	-1.60 e$^-$002	-2.80 e$^-$003				
3.10 e$^-$002	1.57 e$^-$002	-2.60 e$^-$003				
3.09 e$^-$002	1.52 e$^-$002	-2.59 e$^-$003	3.62 e$^-$003	1.79 e$^-$001	1.63 e$^-$001	8.00 e$^-$004
3.21 e$^-$002	1.79 e$^-$002	-2.71 e$^-$003	Er: -2.90 e$^-$002	Er: -2.63 e$^-$003		
3.34 e$^-$002	-1.62 e$^-$002	-2.87 e$^-$003				
3.08 e$^-$002	1.54 e$^-$002	-2.57 e$^-$003				
3.11 e$^-$002	-1.63 e$^-$002	-2.62 e$^-$003				
3.15 e$^-$002	-1.60 e$^-$002	-2.66 e$^-$003				

TABLE X. ENERGY DISSIPATION OF 8x8 VM

$E_{btx}(eV)$	$E_{ctx}(eV)$	$E_{Etx}(eV)$	$S_b(eV)$	$A_b(eV)$	$S_c(eV)$	$A_c(eV)$
1.25 e$^-$001	-6.35 e$^-$001	-1.31 e$^-$002				
1.10 e$^-$001	-6.28 e$^-$001	-1.16 e$^-$002				
2.42 e$^-$001	8.22 e$^-$001	-2.62 e$^-$002				
2.42 e$^-$001	-8.22 e$^-$001	-2.62 e$^-$002				
1.10 e$^-$001	-6.28 e$^-$001	-1.16 e$^-$002	1.79 e$^-$001	1.63 e$^-$001	2.77 e$^-$001	2.52 e$^-$002
1.25 e$^-$001	-6.35 e$^-$001	-1.31 e$^-$002	Er: -1.92 e$^-$002	Er: -1.75 e$^-$002		
1.78 e$^-$001	-4.16 e$^-$001	-1.91 e$^-$002				
1.78 e$^-$001	4.16 e$^-$001	-1.91 e$^-$002				
1.25 e$^-$001	6.35 e$^-$001	-1.32 e$^-$002				
1.10 e$^-$001	-6.28 e$^-$001	-1.16 e$^-$002				
2.42 e$^-$001	-8.22 e$^-$001	-2.62 e$^-$002				

It was also observed that there are 57.14%, 55.55%,48.45%, 28.03% and 42.57% improvements in the area of the HA Circuit, 2×2 VM, 4-bit RCA, 4×4 VM and 8×8 VM circuits respectively. Hence, it can be concluded that the suggested designs exhibit remarkable efficiency concerning number of cells utilized to construct circuit, clock latency, occupied area, and Quantum cost in comparison to previously proposed designs.In the future, the proposed designs will be used to design optimum digital signal processing and nano-communication devices.

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