



Analysis of Reliability for the Gate Level Fault Tolerant Design using Probabilistic Transfer Matrix method

D.Manimekalai¹ and Pradipkumar Dixit²

¹Department of Electrical and Electronics Engineering, Jain University, Bangalore, India

²Department of Electrical and Electronics Engineering, M.S.Ramaiah Institute of Technology, Bangalore, India

Received 23 Mar. 2017, Revised 9 Jul. 2017, Accepted 8 Aug. 2017, Published 1 Sep. 2017

Abstract: As semiconductor integrated circuits entered into nanometer dimensions, large variations of parameters and drastic reduction in reliability conditions of the constituent devices may be expected. On basis of these unreliable concerns, the research in fault analysis and development of fault tolerant design methodologies are the growing concern nowadays. Design and development of the fault tolerant model of the system/circuit include two major areas. First, types of fault and the level of fault occurrence at the input and output of the circuit. Second, the analysis of reliability for the logic circuit. The aim of this paper is to improve the reliability and fault tolerance level of the logic circuit by introducing gate level redundancy with respect to the occurrence of transient fault. Triple Modular Redundancy methodology is used to design the fault tolerant model that improves the reliability of the logic circuit. The proposed Probability Transfer Matrix (PTM) algorithm evaluates and compares the reliability of the logic circuit without redundancy and with redundancy by the analytical formulations. The results of circuit reliability with respect to the gate error probability has been simulated for the occurrence of transient faults for the proposed logic circuits. The results have shown better improvement in reliability and fault tolerance level of 0.7% for the proposed logic circuit using gate level redundancy.

Keywords: Fault tolerance, Single Event Upset, Reliability, Redundancy

1. INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) technology scaling down to nanometer regime for digital and analog circuits leads to unreliable conditions. These reliability problems arise due to the greater variations in parameters, voltage or current thresholds, power consumption and dissipation etc. [1]. The causes for these problems are the process variations such as random dopant fluctuations, gate oxide breakdown, hot carrier injection, bias temperature instability etc., which occur in CMOS devices and electronic circuits [2]. Hence nano scaled components and electronic devices have uncertainty operational conditions under high temperature and external random noise. This leads to the research and development in the area of reliability analysis and reliability based design for the nano scaled electronic circuits. So, the idea in this paper is to get better reliable circuit design by involving redundancy. For the redundancy, a suitable fault tolerant design should be selected such that the redundant design should achieve better reliability. Various fault tolerant

design methodologies and the algorithms are briefly reviewed below.

Ran Xiao et. al [3] reviewed few methods for reliability analysis on gate-level circuits by considering the size and topology (way of gate connections) of the logic circuit. Their paper also analysed the reliability for those circuits with reconvergent fanouts. They proved that, Probability Transfer Matrix (PTM) method and Probabilistic Gate Model (PGM) can provide the exact result for those circuits with reconvergent fanouts. Simulation based methods such as Monte Carlo (MC) simulation and Stochastic Computation Model (SCM) provides the high level of accurate results by the determination of number of simulation runs statistically. They reviewed that all these methods seem to be effective for specific circuits due to the nature and complexity of the reliability analysis problem. In our paper, we used PTM method for analysing the reliability for the proposed logic circuit.

Jie Han et.al [4] used Probabilistic Gate Model (PGM) for the evaluation of reliability. The PGM algorithms evaluate the circuit reliability for each input vector combination and each output. They have shown



the simulation results on LGSynth91 and ISCAS85 benchmark circuits for the values of reliability and execution time using simple PGM and accurate PGM algorithm. They proved that the accurate PGM algorithm could evaluate accurate reliability. This PGM algorithm requires exponential time complexity and computation complexity which increases with respect to the number of gates and the number of reconvergent fanouts in the logic circuit. To overcome the time complexity, this paper proposed PTM algorithm for the estimation of reliability of the 2 input NAND logic circuit which comprises several number of NAND2 logic gates.

Smita et.al [5] developed a general framework based on Probability transfer matrices (PTMs) of the gates to evaluate the circuit reliability based on the soft or transient errors. They incorporated Algebraic Decision Diagrams (ADD) to improve the efficiency of PTM algebraic calculations. They analyzed the circuit reliability for the various benchmark circuits from the gate PTM to circuit PTM.

Denis Teixeira et.al [6] presented the reliability analysis methodologies based on signal probability and they proposed methodology which computes signal reliability as a function of logical masking capabilities by considering multiple simultaneous faults occurrence. After the computation of signal probability, three heuristic algorithms have been proposed namely weighted averaging algorithm, the multi-pass algorithm and the dynamic weighted averaging algorithm. That reduces the effects of reconvergent fanouts by analyzing and comparing the trade-offs between accuracy and execution time. They proved that, the better results are obtained with the multi-pass algorithm for larger circuits. This paper considers the input signal probability based on the transient fault which occur due to the change in environmental conditions, for the analysis of reliability and fault tolerance.

Tejinder singh et.al [7] designed and analysed the 4-bit Arithmetic and Logic Unit (ALU) circuit using CMOS 180nm process technology for fault tolerant computing structures. They used the fault tolerant technique known as Triple Modular Redundancy (TMR) to tolerate the manufacturing defects which achieves higher reliability. They also calculated the power consumption results for all the arithmetic and logical operations. In this paper, we also used the TMR technique to tolerate the transient or permanent faults that occur at the input signals and lines for the NAND2 logic circuit.

Walid Ibrahim et.al [8] analyzed the trade-off between reliability and power, area and delay parameters using the optimum sizing method. The simulation results proved the improvement of the reliabilities of INV, NAND-2 and NOR-2 by the factors of more than 10^5 , 10 and 10^{10} respectively. This paper analyse the trade-off

between the circuit reliability and the gate error probability given the input signal probability using Probability Transfer Matrix (PTM) method.

The paper is organized as follows. The causes of transient fault and the importance of gate level redundancy is given in section 2. In section 3, the proposed fault tolerant design is described generally, followed by the functional description of the proposed NAND2 network. The description of PTM method and the analysis of reliability for the proposed logic circuit is illustrated in detail under section 4. Simulation results of reliability vs gate error probability for three forms of NAND2 circuits has been discussed in section 5, followed by the conclusion in section 6.

2. GATE LEVEL REDUNDANCY

Due to shrinking down dimensions of supply voltage/current, SiO₂ thickness, channel length and width, doping concentration and capacitance, various reliability problems arise for the CMOS devices. The reliability problems have to be considered are faults and defects which lead to failure or inoperable state of the system/circuit. Fault is a critical defect which affects the operation of the circuit. In general, faults can be broadly classified as permanent, transient and intermittent faults. Permanent faults remain stable until a repair or replacement is undertaken. Transient or soft faults occur for a short period of time and this do not lead to permanent damage. Intermittent faults occur first which eventually tends to be permanent [9].

The soft error arises from Single Event Upset (SEU) and that are more susceptible to semiconductor integrated circuits due to the scaling down technology [10]. A Single Event Upset (SEU) is a change of output state caused by striking of high speed neutron and alpha (charged) particles such as electrons, protons etc. in integrated circuits. When the electrons or protons travels through the different regions and nodes in a switching device, the ionization path will be created which results in recombination of electron hole pairs in many regions. The ionization path consist of free electrons and holes. When the path penetrates to the depletion region, the free electrons in the path will be attracted to a high voltage NMOS drain diffusion, which results in the change of output of the NMOS switching device. Similarly, the holes will be attracted to a low voltage PMOS diffusion for PMOS transistors. [11]. The state of output changes due to the charged particles created by ionization in the node of a logic element (e.g. memory "bit"). Totally, an SEU is the error in device output or operation due to the particle strike.

The appropriate fault tolerant design methodologies are required for any nano scaled systems to tolerate these single event effects. The one and only technique for fault

tolerant design to improve the reliability is the addition of redundancy. Redundancy methodologies are incorporated to model the fault tolerant system/circuit with the negation of the effects of failure. There are three kinds of redundancy listed as time redundancy, space redundancy and information redundancy. Time redundancy repeat computations during specific period of time. In information redundancy, the bit errors in a data can be detected, coded and corrected by the use of error-detection and error-correction codes [12]. Finally, space redundancy depends on the number of devices or gate combinations located in a system/circuit. This space redundancy is developed at three different levels in the digital system such as circuit, gate and transistor level.

SEU analysis and circuit reliability evaluation can be carried out at gate level and transistor level. Gate level probabilistic models are designed based on the type of gates located in the circuit and the topological interconnections (serial or parallel, reconvergent fanouts) between the gates in the logic circuit [13]. Some of the probabilistic methods are Two Pass (TP) Algorithm, Signal Probability Algorithm (SPRA), Probabilistic Transfer Matrix (PTM) Algorithm etc. Transistor level methods include simulation based fault injection and statistical analysis to analyze the output error and circuit reliability [14].

On above considerations, the objectives of the paper are sequentially listed below:

1. In this paper, the transient fault is modelled as bit flip change at the input signal patterns for the proposed NAND2 logic circuits.
2. Gate level redundancy is taken as consideration to design the relevant fault tolerant model based on the transient faults which occur at the input vector combinations in the logic circuits.
3. The paper focusses on the design of Gate level probabilistic model and analyses the reliability using Probabilistic Transfer Matrix (PTM) method for the proposed logic circuits.
4. Using PTM method, the analysis of reliability for the NAND2 logic circuit should be determined through the simulation runs of circuit reliability given the gate error probability.

3. PROPOSED DESIGN

Redundancy provides the allocation of additional components, functions and the required input data for the entire system/circuit which could give the correct functioning of output in spite of the presence of faults in the system/circuit. Therefore, the faults could be tolerated or masked by the various kinds of fault tolerant techniques such as Triple Modular Redundancy (TMR), N-modular Redundancy (NMR), Cascaded Triple Modular Redundancy (TMR), NAND Multiplexing technique etc [15].

A. Fault Tolerant Design

In this paper, TMR technique is proposed to tolerate the faults, which might occur due to various process variations in the logical gates and circuits. The general block diagram of TMR system is given below in Figure (1)

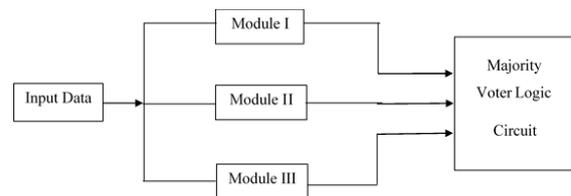


Figure 1. Block Diagram of TMR System

In general, TMR system comprises of two units. The first unit is the triple modules (i.e) the triplication of identical system/circuit in parallel composition as three sub modules that contain the same data input and could perform the same function at the same time [11]. The reliability of TMR technique of the system is given by the probability that the circuit should perform the same functional operation at the same time as like reliability of each module R_{mod} . The second unit of TMR system is the majority voter logic circuit. The output of the three sub modules are fed as input for the voter logic circuit. The voter logic circuit comprises of three number of AND gates for which, the inputs are the outputs from three sub modules and one OR gate. This voting logic unit can mask the faulty module by comparing the output of the three sub modules whether all the three outputs are same or two modules output are same. If three modules output are same, the voter will select the same output which shows that there is no fault occurrence. If two of the three modules output are same, the voter will select the majority output i.e. this voter could mask one faulty module. If one module fails, the other two will outvote it and the voter output remains correct. Therefore, the reliability of voter logic unit is represented as R_{VOT} .

Therefore, the reliability of triple modular redundant circuit is equal to the multiple of the probability of having at least 2 out of 3 instances of TMR and it is denoted as R_{TMR} . So, R_{TMR} can be determined from the reliability values of each module R_{mod} with the index k value of at least 2 out of total 3 modules and the reliability of voter logic unit R_{VOT} as given in (1).

$$R_{TMR} = R_{VOT} \cdot \sum_{k=2}^3 \binom{3}{k} R_{mod}^k (1 - R_{mod})^{3-k} \quad (1)$$

After simplifying, we get (2) as,

$$R_{TMR} = R_{VOT} \cdot [3R_{mod}^2 - 2R_{mod}^3] \quad (2)$$

B. NAND2 Circuit Logic Design

The proposed NAND2 circuit configuration for the analysis of reliability and fault tolerance is shown in Figure 2. It consists of three blocks of NAND2 gates which is arranged in the sequence of $gn^2: gn : gn^0$ where gn can be considered as the value 2 as it consist of 2 input NAND gates. Therefore, BLOCK III consist of four number of NAND2 gates, BLOCK II consist of two number of NAND2 gates followed by only one NAND2 gate in BLOCK I. The output of the proposed example circuit is same as the single two input NAND gate. This circuit configuration can be extended to 5 blocks or 7 blocks which could be arranged in the sequence of $gn^4 : gn^3 : gn^2 : gn : gn^0$ or $gn^6 : gn^5 : gn^4 : gn^3 : gn^2 : gn : gn^0$.

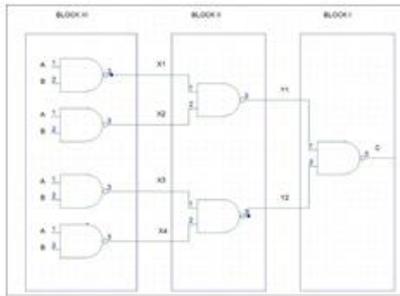


Figure 2. NAND2 Circuit Network

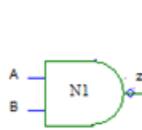


Figure 3.(a) Circuit I

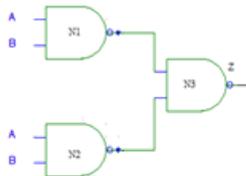


Figure 3.(b) Circuit II

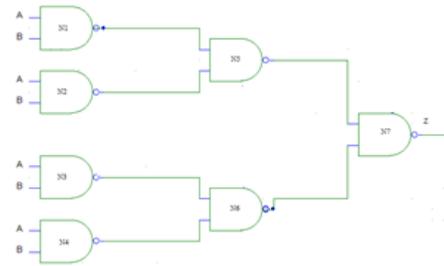


Figure 3.(c) Circuit III or Whole NAND2 Circuit

In this paper, we modelled this NAND2 circuit network as three number of NAND2 circuits for the analysis of reliability by introducing triple modular redundancy. Circuit I shown in Figure 3.(a) is the single NAND2 gate i.e only BLOCK I from NAND2 network followed by Circuit II which is designed by three number of NAND2 gates i.e BLOCK I associated with BLOCK II and Circuit III is the whole NAND2 network consist of seven NAND2 gates i.e., the whole NAND2 network circuit. Circuit II and III are represented in Figure 3.(b) and 3.(c) respectively.

4. ANALYSIS OF RELIABILITY USING PROBABILITY TRANSFER MATRIX ALGORITHM

For each circuit, gate level redundancy is applied by introducing the redundant components/circuits. This paper uses the Triple Modular Redundancy (TMR) technique to design the fault tolerant model and Probability Transfer Matrix (PTM) method is used to evaluate and analyse the reliability of all the NAND2 circuits. The overall combinational circuit reliability, termed as R_{ckt} is the function of gate reliability R_g and the input signal Probability P_{in} . Therefore R_{ckt} can be defined in (3) as,

$$R_{ckt} = f(R_g, P_{in}) \quad (3)$$

In this paper, the gate error Probability denoted as P_g in (4) is given as the subtraction of gate reliability R_g from the total probability or unit and it is given as,

$$P_g = 1 - R_g \quad (4)$$

A. PTM Algorithm

PTM method is an algorithm which can be used to analyze the reliability of the circuit accurately. This method is used to evaluate the reliability for the entire circuit probabilistically. In this paper, we analyze the circuit reliability and various signal probabilities using PTM. In general, a PTM of the circuit or gate is defined as the probability of each output combination with respect to the corresponding input signal patterns.

For instance, if single NAND gate experiences the error probability p , then the gate's PTM denoted as M_g and is defined in (5) as,

$$M_g = \begin{matrix} & 0 & 1 \\ \begin{matrix} 00 \\ 01 \\ 10 \\ 11 \end{matrix} & \begin{bmatrix} p & 1-p \\ p & 1-p \\ p & 1-p \\ 1-p & p \end{bmatrix} \end{matrix} \quad (5)$$

The above equation shows that, the row indices represents the input signal patterns and the column indices represents the output signals logic ‘0’ and ‘1’. Each value in matrix M_g states the conditional probability that a certain output logic state occurs given a certain input signal patterns. A fault free gate or circuit’s PTM is defined as the Identity Transfer Matrix (ITM) and it is generally denoted as I. For the fault free NAND gate, the Identity Transfer Matrix I_g in (6) is given by,

$$I_g = \begin{matrix} & 0 & 1 \\ \begin{matrix} 00 \\ 01 \\ 10 \\ 11 \end{matrix} & \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \end{matrix} \quad (6)$$

To evaluate the reliability of the combinational circuits, the probabilities to be considered are the input signal error probability, output error probability and the gate error probability. The input signal error probability is taken as the probability that the erred input vector may occur due to the transient fault i.e bit flip change, in spite of no change in output combination. The output error probabilities are the probabilities that the output error results for each input signal pattern. Each gate in the logic circuit experiences an error known as gate error probability. The gate error probability P_g depends on the input signal patterns or combinations. The main operation needed to compute the circuit reliability is the logic circuit’s Probability Transfer matrix (PTM) which could be determined from the individual gate’s PTM. In this paper, the parameters formulated to determine circuit’s PTM are the gate error probability, both input and output error signal probability. The major computations required to evaluate the circuit reliability and the signal probabilities are matrix multiplications and tensor products. The value of the circuit’s PTM depends on the gate’s topology (connections) in the logical circuit. The logic circuits which are arranged in serial composition or parallel composition require matrix multiplications and tensor products respectively to evaluate the circuit’s PTM.

B. Illustration of PTM Algorithm for the Evaluation and Analysis of Reliability

Step 1: The proposed logic circuit for illustration is shown in Figure.4.(a) and 4.(b). The non-redundant logic circuit shown in Figure 4.(a) is partitioned into

two sections as S1 and S2. S1 section is the parallel composition of two NAND2 gates noted as N1 and N2, whereas S2 section consist of only one 2 input NAND gate N3. Triple modular Redundancy is applied for the logic schematic to tolerate or mask the faults and the corresponding fault tolerant model is shown in Figure 4.(b). Therefore, the TMR circuit consist of two portions. First portion is the triplar unit i.e replication of three modules/circuit and the second portion is the majority voter logic unit. Voter logic unit is partitioned into three sections V1,V2 and V3. Section V1 is the parallel composition of three number of reconvergent fanouts F1,F2 and F3.

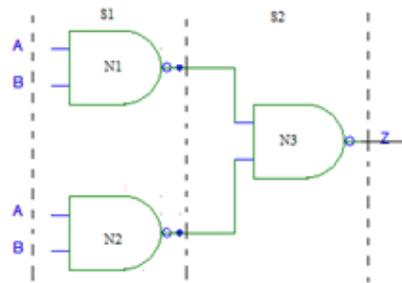


Figure 4.(a). Non Redundant Logic Schematic for Illustration

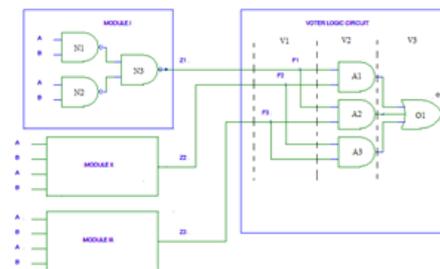


Figure 4.(b). Redundant Logic Schematic for Illustration

Section V2 is the tensoring of three AND gates A1, A2 and A3 followed by section V3 which consist of one 3 input OR gate O1.

Step 2: Assumption and estimation of the input parameters for the reliability analysis of the gate level fault tolerant design for the circuit are defined below:

1. *Gate Error Probability:* It is defined as the probability that each logic gate experiences an error and it is denoted as P_g . The gate error probability P_g is given as $1-R_g$ where R_g the gate reliability is assuming as 0.98. Therefore P_g is 0.02.

2. *Input Signal Error Probability:* Consider the circuit in Figure 4.(a). It consists of three NAND2 gates. The gate N1 has two inputs A and B. The same inputs are

given for the gate N2. So the input signal pattern for the given circuit can be denoted as ABAB. Therefore, four input vector combinations are possible and is listed below in the side of the probability matrix, other input vectors can be discarded out of 16 signal patterns. The input signal error probability is considered as the probability that the erred input vector may occur due to the transient fault i.e bit flip change, in spite of no change in output. For the input vectors “0000”, “0101” and “1010”, the output of the circuit will result as same logic ‘0’. So the signal error probability is estimated as 0.33 for the above three input vectors. For the last input vector “1111”, the result is logic ‘1’. Based on these considerations, the matrix representation for the input signal error probability P_{in} is defined below in (7):

The Input signal error probability

$$P_{in} = \begin{matrix} 0000 \\ 0101 \\ 1010 \\ 1111 \end{matrix} \begin{bmatrix} 0.33 \\ 0.33 \\ 0.33 \\ 0 \end{bmatrix} \quad (7)$$

3. Voter Input Signal Probability: It is denoted as P_{vi} . The output of the voter logic circuit flips to logic ‘1’ from logic ‘0’ for few input signal patterns. The probability is uniformly distributed for those input vector combinations and the corresponding matrix representation is given below in (8):

The Voter logic input signal probability

$$P_{vi} = \begin{matrix} 000 \\ 001 \\ 010 \\ 011 \\ 100 \\ 101 \\ 110 \\ 111 \end{matrix} \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0.25 \\ 0 \\ 0.25 \\ 0.25 \\ 0.25 \end{bmatrix} \quad (8)$$

Step 3: Evaluation of the non-redundant NAND2 circuit PTM.

The Probability Transfer matrix for each NAND2 gate denoted as M_{Ni} is given below in (9)

$$M_{Ni} = \begin{bmatrix} 1 - Rg & Pg \\ 1 - Rg & Pg \\ 1 - Rg & Pg \\ Pg & 1 - Rg \end{bmatrix} \quad (9)$$

Non redundant circuit PTM has been determined from the gate PTMs of section S1 and S2 in the logic circuit shown above in Figure 4.(a). The gate PTMs are tensored together for the parallel composition of N1 and N2 in section S1. The resulting PTM is multiplied with the PTM of the next section S2. Thus, PTM for the non-

redundant circuit denoted as M_{NRED} can be determined from the gate PTMs, M_{N1} , M_{N2} and M_{N3} as per (10),

$$M_{NRED} = (M_{N1} \otimes M_{N2})_{16 \times 4} \cdot (M_{N3})_{4 \times 2} \quad (10)$$

The value of gate reliability ranges from 0.90 to 0.99 for the evaluation of reliability of the NAND2 circuit shown above. The following illustration takes one of the values of gate reliability from the above range as 0.98 and assuming all the gate reliabilities as 0.98, M_{NRED} is solved below in (11) using above (9) and (10) as follows:

$$M_{NRED} = \begin{matrix} 0000 \\ 0001 \\ 0010 \\ 0011 \\ 0100 \\ 0101 \\ 0110 \\ 0111 \\ 1000 \\ 1001 \\ 1010 \\ 1011 \\ 1100 \\ 1101 \\ 1110 \\ 1111 \end{matrix} \begin{bmatrix} 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.0388 & 0.9612 \\ 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.0388 & 0.9612 \\ 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.0388 & 0.9612 \\ 0.0388 & 0.9612 \\ 0.0388 & 0.9612 \\ 0.0388 & 0.9612 \\ 0.0204 & 0.9796 \end{bmatrix} \quad (11)$$

The same inputs are given for gates N1 and N2 in the given circuit. As per the input signal pattern “ABAB”, four input vector combinations are possible out of 16 combinations. So after discarding the impossible values and patterns from (11), M_{NRED} has been simplified as (12). The corresponding Identity Transfer Matrix (ITM) denoted as I_{NRED} is given in (13).

$$M_{NRED} = \begin{matrix} 0000 \\ 0101 \\ 1010 \\ 1111 \end{matrix} \begin{bmatrix} 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.942 & 0.058 \\ 0.0204 & 0.9796 \end{bmatrix} \quad (12)$$

$$I_{NRED} = \begin{matrix} 0000 \\ 0101 \\ 1010 \\ 1111 \end{matrix} \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (13)$$

Step 4: Determination of Reliability for non-redundant NAND2 circuit.

The reliability for the combinational circuit R_{ckt} is the function of gate reliability and the input signal probability P_{in} from (3). Circuit’s PTM is defined as the function of reliability and the input signal probability matrix is defined above in (7).



Therefore the reliability of the circuit is determined in (14) as,

$$R_{ckt} = \sum_{i,j}^{INRED(i,j)=1} M_{NRED}(i,j) P_{in}(i) \quad (14)$$

By using (12), (13) and (14), the reliability of the non-redundant NAND2 circuit R_{NRED} is calculated and it is given in (15),

$$R_{NRED} = 0.9326 \quad (15)$$

Step 5: Evaluation of PTM for Redundant logic circuit shown in Figure 4.(b)

The circuit can be named as TMR circuit, that comprises of both the triple modular unit and the voter logic unit and the corresponding PTM's are denoted as M_{mod} and M_{VOT} respectively.

For the Triple Modular unit, the PTM M_{mod} is found in (16) as,

$$M_{mod} = \begin{matrix} 0000 & 0.8359 & 0.0515 & 0.0515 & 0.0032 & 0.0515 & 0.0032 & 0.0032 & 0.0002 \\ 0101 & 0.8359 & 0.0515 & 0.0515 & 0.0032 & 0.0515 & 0.0032 & 0.0032 & 0.0002 \\ 1010 & 0.8359 & 0.0515 & 0.0515 & 0.0032 & 0.0515 & 0.0032 & 0.0032 & 0.0002 \\ 1111 & 0.0000 & 0.0004 & 0.0004 & 0.0196 & 0.0004 & 0.0196 & 0.0196 & 0.9401 \end{matrix} \quad (16)$$

Therefore, the reliability for each module R_{mod} is estimated in (17),

$$R_{mod} = 0.9326 \quad (17)$$

For the Majority Voter Logic Circuit, PTM noted as M_{VOT} is determined in (19) from the sections PTM of V1, V2 and V3 as given in (18)

$$M_{VOT} = M_{V1} \cdot M_{V2} \cdot M_{V3} \\ M_{VOT} = (F_1 \otimes F_2 \otimes F_3)_{8 \times 64} \\ \cdot (M_{A1} \otimes M_{A2} \otimes M_{A3})_{64 \times 8} \\ \cdot (M_{O1})_{8 \times 2} \quad (18)$$

$$M_{VOT} = \begin{matrix} 000 & 0.9062 & 0.0938 \\ 001 & 0.0381 & 0.9619 \\ 010 & 0.0565 & 0.9435 \\ 011 & 0.0207 & 0.9793 \\ 100 & 0.0565 & 0.9435 \\ 101 & 0.0207 & 0.9793 \\ 110 & 0.0392 & 0.9608 \\ 111 & 0.0204 & 0.9796 \end{matrix} \quad (19)$$

R_{VOT} is determined from M_{VOT} and is given in (20),

$$R_{VOT} = 0.9747 \quad (20)$$

Step 6: Determination of Reliability for the redundant NAND2 circuit.

The values of R_{mod} and R_{VOT} are substituted in (2). Therefore the reliability for the TMR or Redundant NAND2 circuit termed as R_{TMR} has been determined and is given below in (21),

$$R_{TMR} = 0.9620 \quad (21)$$

By comparing (15) and (21), it can be analysed that the reliability for the redundant circuit is improved than

for the non-redundant circuit. This result shows that the fault could be tolerated and the circuit could maintain the same operation time and level to certain instant.

5. SIMULATION AND DISCUSSION

The simulation results shows the comparison of reliability for the non-redundant and TMR redundant NAND2 circuit with respect to various levels of gate error probability for three NAND2 circuit model as shown in Figure 3.(a), 3.(b) and 3.(c).

The Figure 5.(a) shows the comparison of circuit reliability values for non-redundant and redundant TMR circuit for Circuit I shown in Figure 3.(a), which consist of single NAND2 gate. When the TMR technique is applied for Circuit I, it is analysed that for Triple Modular Redundant circuit, the values of circuit reliability has increased when compared to the non-redundant circuit for the level of gate error probability ranges from 0.01 to 0.023. When the gate error probability exceeds above 0.024, the reliability for non-redundant NAND2 gate becomes greater when compared to the redundant TMR circuit. From this, it can be analyzed that, the Circuit I can tolerate 2.4% of gate error during the functional operation conditions.

From Figure 5.(a), it is also analysed when the TMR technique is applied and designed for Circuit I, the value of circuit reliability has increased from 0.98 to 0.986. It shows that the better improvement in the circuit reliability and maximum fault tolerance level of 0.6% is achieved at the initial level of gate error probability of 0.01 for Circuit I.

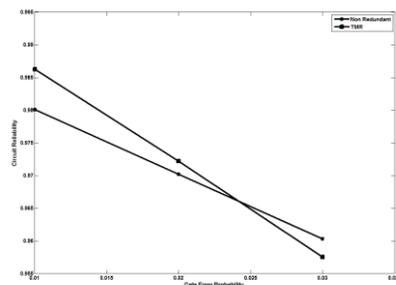


Figure 5.(a) Analysis of Circuit I

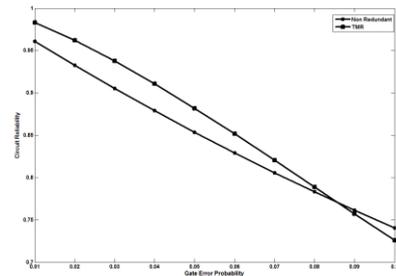


Figure 5.(b) Analysis of Circuit II

The figure 5.(b) shows the analysis of reliability values for non-redundant and redundant TMR model for circuit II as shown in Figure 3.(b) which consist of three NAND2 gates. By using the gate level TMR technique for Circuit II, it is shown that for TMR circuit, the values of circuit reliability has increased when compared to the circuit reliability values of non-redundant circuit for the level of gate error probability ranges from 0.01 to 0.084. When the gate error probability exceeds above 0.085, the reliability for non-redundant NAND2 gate becomes greater when compared to the redundant TMR circuit. This shows that for Circuit II, gate can tolerate the error upto 8.5%. It is also analysed that when the TMR technique is used and designed for Circuit II, the value of circuit reliability has increased from 0.9 to 0.932 at the gate error probability of 0.03. It shows that the better improvement in the circuit reliability and maximum fault tolerance level of 3.23% is achieved for the level of gate error probability of 0.03 for Circuit II.

The figure 5.(c) shows the analysis of reliability values for non-redundant and redundant TMR model for the total NAND2 network circuit shown in Figure 3.(c) which consist of seven NAND2 gates. By applying the gate level TMR technique for the whole NAND2 circuit, it is shown that for TMR circuit, the values of circuit reliability has increased when compared to the circuit reliability values of non-redundant circuit for the level of gate error probability ranges from 0.01 to 0.039. When the gate error probability exceeds above 0.04, the reliability for non-redundant NAND2 gate becomes greater when compared to the redundant TMR circuit. This shows that for total NAND2 circuit, each gate can tolerate the error upto 4%. It is also analysed that when the TMR technique is used and designed for whole NAND2 circuit, the value of circuit reliability has increased from 0.98 to 0.987 at the initial level of gate error probability of 0.01. It shows that the better improvement in the circuit reliability and maximum fault tolerance level of 0.7% is achieved for the level of gate error probability of 0.01 for total NAND2 Network circuit.

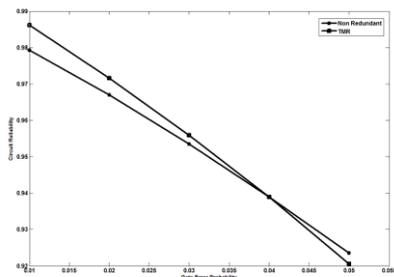


Figure 5.(c) Analysis of Circuit III

6. CONCLUSION

On the basis of CMOS technology scaling considerations, this paper focused on the reliability analysis for the nano-scaled logic circuits using Probability Transfer Matrix (PTM) algorithm. Firstly, the fault tolerant model has been designed by adding Triple Modular Redundancy (TMR) methodology with respect to the occurrence of transient fault at the input signal patterns for the proposed NAND2 Logic schematics. Secondly, the reliability of three forms of non-redundant and redundant NAND2 logic schematics has been evaluated and analysed based on PTM algorithm. Finally, the analytical formulations of PTM has been simulated and analysed for the comparison of reliability for NAND2 circuits without redundancy and with redundancy. The results have shown the improvement in reliability for the redundant logic circuit. The PTM method gives accurate results for the circuits with reconvergent fan-outs, but this method requires the space complexity due to the calculation of many tensor products of matrices.

REFERENCES

- [1] Nanditha P. Rao and Madhav P. Desai, "Higher likelihood of multiple bit-flips due to neutron-induced strikes on logic gates", arXiv:1612.08239v1 [cs.AR] 25 Dec 2016, pp. 1-6.
- [2] Zhiming Yang, Junbao Li, Yang Yu and Xiyuan Peng, "NBTI-Aware transient fault rate analysis method for logic Circuit based on probability voltage transfer characteristics", MDPI Algorithms – Open Access Journal, Vol. 9, pp. 1-14, 2016.
- [3] Ran Xiao and Chunhong Chen, "Gate-level circuit reliability analysis: A survey", Hindawi Publishing Corporation VLSI Design, Vol.2014, pp.1-12, 2014.
- [4] Jie Han, Hao Chen, Erin Boykin and Jose Fortes, "Reliability evaluation of logic circuits using probabilistic gate models", Microelectronics Reliability, Vol.51, pp.468-476, 2011.
- [5] Smita Krishnaswamy, George F. Viamontes, Igor L. Markov and John P. Hayes, "Accurate reliability evaluation and enhancement via probabilistic transfer matrices", in Proceedings of the Design Automation and Test in Europe, Vol.1, pp. 282-287, 2005.
- [6] Denis Teixeira Franco, Maí Correia Vasconcelos, Lirida Naviner and Jean-François Naviner, "Signal probability for reliability evaluation of logic circuits", Microelectronics Reliability, Vol. 48, pp. 1586–1591, 2008.
- [7] Tejinder Singh, Farzaneh Pasaie and Rajat Kumar, "Redundancy based design and analysis of ALU Circuit using CMOS 180nm Process Technology for fault tolerant computing architectures", International Journal of Computing and Digital Systems, Vol. 4, No. 1, pp. 53 – 62, 2015.
- [8] Walid Ibrahim, Valeriu Beiu and Azam Bag, "Optimum reliability sizing for complementary metal oxide semiconductor gates", IEEE Transactions on Reliability, Vol. 61, No. 3, pp. 675-686, 2012.
- [9] Natasa Miskov-Zivanov and Diana Marculescu, "Circuit reliability analysis using symbolic techniques", IEEE

Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 25, No. 12, pp. 2638-2649, 2006.

- [10] Natasa Miskov-Zivanov and Diana Marculescu, "Multiple transient faults in combinational and sequential circuits: A systematic approach", Vol.5847, pp.1- 14,2010.
- [11] San Jose," Introduction to Single-Event Upsets", Altera Corporation, www.altera.com, pp. 1-9, 2013
- [12] Walid Ibrahim and Valeriu Beiu, " Using bayesian networks to accurately calculate the reliability of complementary metal Oxide Semiconductor Gates", IEEE Transactions on Reliability, Vol. 60, No. 3, pp. 538-549, 2011.
- [13] S. Krishnaswamy, "Design, analysis and test of logic circuits under uncertainty, Lecture Notes in Electrical Engineering, Springer Science + Business Media , pp. 21-36, 2013.
- [14] Wang zhen, Jiang Jianhui and Yang Guang, , "Implementation and analysis of probabilistic methods for gate-level circuit reliability estimation", Tsinghua Science and Technology, Vol.12. pp. 32-38, 2007
- [15] Milos Stanisavljevic, Alexandre Schmid and Yusuf Leblebici, "Optimization of nanoelectronic systems reliability under massive defect density using Distributed R-fold Modular Redundancy(DRMR)",IEEE Computer Society, 24th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2009.



D.Manimekalai is a research Scholar doing Ph.D in Jain University, Bangalore. She received her Bachelor of Engineering degree in Instrumentation and Control from Arulmigu Kalasalingam College of Engineering, Madurai Kamaraj University in 2001 and Master of Engineering in Industrial Engineering from Thiagarajar College of Engineering, Anna University in 2005. Her research interest includes Low power VLSI Design, Characterization of Nano scaled CMOS circuits and systems, design and analysis of reliability of Nano systems.



Pradipkumar Dixit was born in Bijapur, Karnataka, India in 1964. He received the BE degree in Electrical and Electronics Engineering from Mysore University in 1989 and M.Tech. degree in Power and Energy Systems from NITK, Surathkal, Mangalore University, India in 1995 and the Ph.D. degree from Visvesvaraya Technological University, Belgaum, India in 2010 for his thesis titled "Studies on Pollution Performance of Ceramic Insulators". Currently, he is working as Professor & Head in the department of Electrical and Electronics Engineering, M. S Ramaiah Institute of Technology, Bangalore, Karnataka, India. His research interests include outdoor insulation, insulation engineering and artificial intelligence to electrical engineering.