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Field Programmable Gate Array System for IoT Applications

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Abstract: Internet of Things (IoT) becomes an attractive field of research in the last decade. The main objective of IoT is enabling the integration and interconnection of the physical world and the cyber space. The aim of such space is telecommunications of the online world of computer networks and the Internet. The recent advances in sensors network and embedded systems have helped in the development and realization of Internet of Things. In order to provide adapted services to the users, such spaces should operate in a proactive manner and according to the current context. A Field Programmable Gate Array (FPGA) is a programmable chip designed to be configured after manufacturing by a designer or a customer using special computer interface hardware tools. The FPGA configuration is generally specified using a Hardware Description Language (HDL), there are many applications nowadays that are using FPGA-based design as the main controller instead of using ASICs (Application Specific Integrated circuits) design. This paper presents the hardware implementation of an FPGA (Field Programmable Gate Array) based design for IoT (Internet of Things) applications. The main contribution in this paper is to introduce a cost effective design to be used for the applications of IoT, the FPGA based design has been described using VHDL (VHSIC Hardware Description Language), simulated using Xilinx ISE 14.7 software tools, and then implemented on Xilinx Virtex-7 FPGA VC707 Evaluation platform, targeting xc7vx485t-2ffg1761 device.

Keywords: FPGA; GSM; IoT; ASICs; VHDL.

1. INTRODUCTION

The rapid Internet of Things (IoT) is the world of connecting millions of different physical devices together through the internet. IoT makes it possible to remotely access different type of actuators in long distance through the internet, as well as controlling physical devices also in long distance through the internet [1-3]. The term "Things" in the IoT refer to a wide variety of devices such as health monitoring devices, environmental and climate control and monitoring devices, and intelligent transportation systems devices. Examples of IoT are given in Fig. 1, 2, and 3. Humidity and temperature are considered to be the two climate control principles [4]. Humidity affects growth of greenhouse crops mainly through its impact on leaf size and light interception rather than through a direct impact on photosynthesis by increasing the stomata conductance at low VPD (Vapor this sense, programmable Logic Devices (PLDs) present as a good option for the technology development and implementation, because PLDs allow fast development of prototypes and the design of complex hardware systems using FPGAs (Field Programmable Gate Arrays) and Complex Programmable Logic Devices [9-11]. Real-time monitoring provides reliable, timely information of crop and soil status, important in taking decisions for crop production improvement [12-15]. Evaluation of agricultural production systems is a time consuming and difficult process because it means performing visits to selected crop fields to be able to measure and register certain physical, chemical and biological characteristics of the cultivated areas [16-18] . GSM provides a reliable and 24 hours remote monitoring system [19-22].

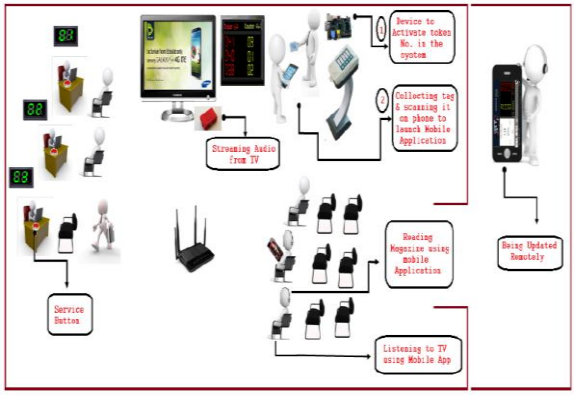

Figure 1. Overall System Diagra[23, 24]

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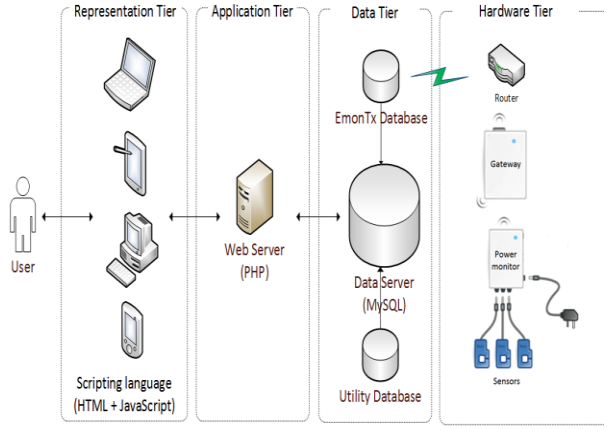

Figure 2. Architectural Design of the iTrack System [25]

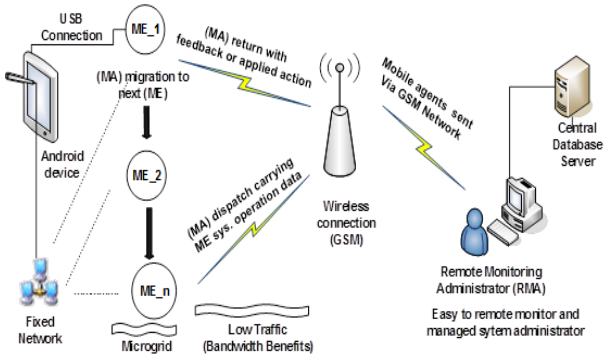

Figure 3. Proposal for data transfer process for decentralized energy system through mobile network based on MA [26]

This research introduces a field programmable gate array system that can be used for IoT Applications in the real time. The main advantage of using FPGA platform is the large number inputs and outputs interface pins available in the FPGA compared to other platforms, especially the selected target device has 1761 I/O pins. The design has been synthesized, simulated, and then implemented using Xilinx ISE design suite 14.7, at the end the design has targeted a Xilinx virtex xc7vx485t-2ffg1761 FPGA. The Virtex-7 FPGA VC707 evaluation platform is a fully featured, highly flexible, and high speed serial base platform. It includes IP cores, and advanced memory interfacing. The materials in this article are organized as follows: following the introduction section is the FPGA-GSM interface, which is discussed in section 2, in section 3 we will discuss the simulation results and design summary; section IV gives a conclusion about the work presented in this paper and the future work.

2. FPGA-GSM INTERFACE

In this section we are going to describe the system architecture design and the FPGA-GSM interfacing. The architecture of the system mainly consists of three components, the GSM MODEM, the controller, and the interface circuit that include the different actuators. The function of the GSM MODEM is the remote communication between the user and the controller through the RS232 serial communication standard. The function of the controller is to continuously check the inputs coming from the different actuators and communicate through the GSM network in case of emergency such that it acts as a 24 hours monitoring, and continuously checking for any received message from the user through the GSM MODEM to switch on or off a selected device. The control centre in turn consists of two units; the PC and mobile phone connected together serially through the RS232 communication port. The system board consists of three units; the controller unit which has been implemented in Virtex-7 FPGA VC707 Evaluation platform given in Fig. 4, the sensor circuit, and the GSM (Global System for Mobile) modem, the controller connected to the GSM modem through the serial communication port as shown in Fig. 4.

Figure 4. Virtex-7 FPGA VC707 Evaluation platform

As an applications for temperature and humidity sensing, the main function of system board in that case is continuously measure the temperature and humidity and compares the measured values with a threshold level, and sends message through GSM network to the control center in case of high temperature or humidity exceeds the threshold level. The main subunit of the system board is the controller that has been designed using VHDL and tested using Xilinx Virtex-7 FPGA VC707 Evaluation platform. Fig. 5 shows a block diagram of the system board that shows the subunits of the controller with connections to the GSM modem and the sensors circuits are indicated. The controller has many components; the most important components that we will describe here are the CU (Control Unit), the ROM memory, the HMU (Humidity Measurements Unit), and the TMU

(Temperature Measurements Unit). Each component has its own inputs, the input for the HMU is coming from the humidity sensor circuit, and the TMU input is coming from the temperature sensor circuit. The HMU and TMU send control signals to CU in case of low humidity or high temperature. The main function of the CU is to send message through the GSM network to the control center according to the given signals coming from the HMU and TMU units. In some cases the CU can take action according to the given data coming from the HMU and TMU units, for example for high temperature it can turn on the fans. In the following section we are going to show the simulation results for each of the four components. The FPGA to GSM design interface has been described using VHDL, synthesized using Xilinx ISE tools; the generated Register Transfer Level (RTL) Schematic for GSM Interface Unite is shown in Fig. 6.

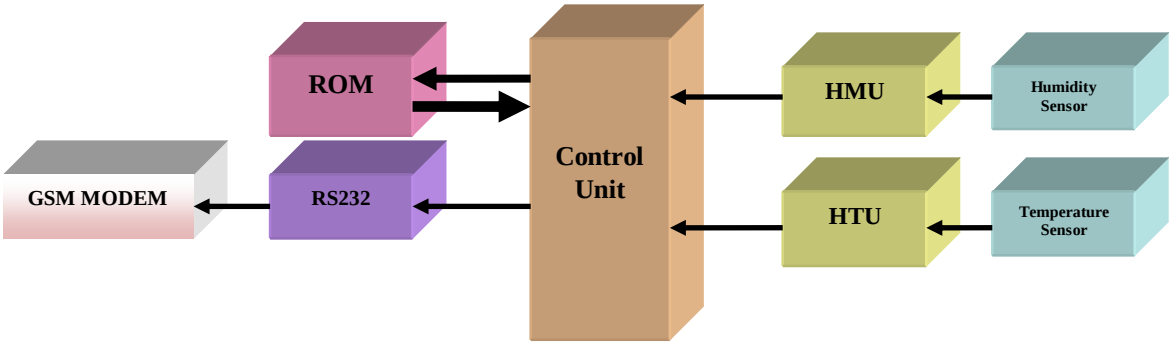

Figure 5. Block Diagram for the System Board

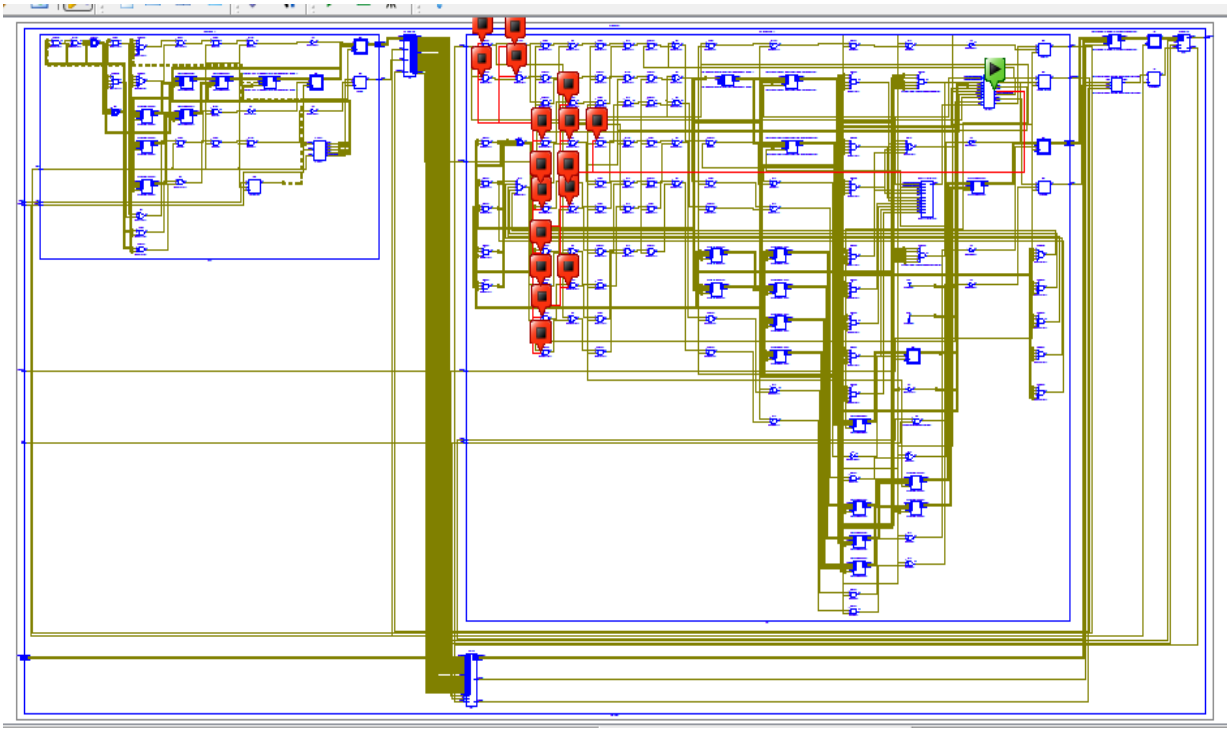

Figure 6. RTL Schematic for GSM Interface Unite

Fig. 7 shows the top level module of the storage unit (U2), the complete RTL schematic of the storage unit is shown in Fig. 8, and a zooming in of different parts of the RTL schematic are given in Fig. 9 and 10.

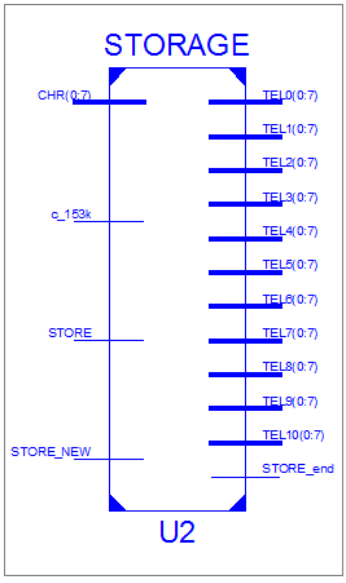

Figure 7. Top level module of the storage unit

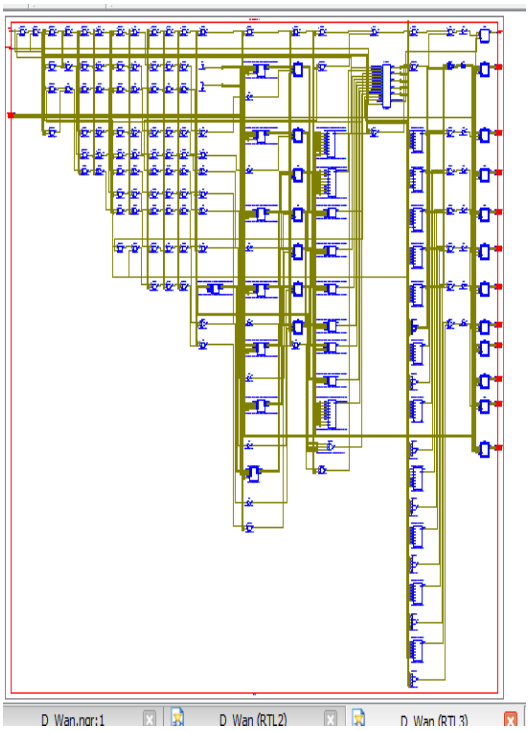

Figure 8. Complete RTL schematic of the storage unit

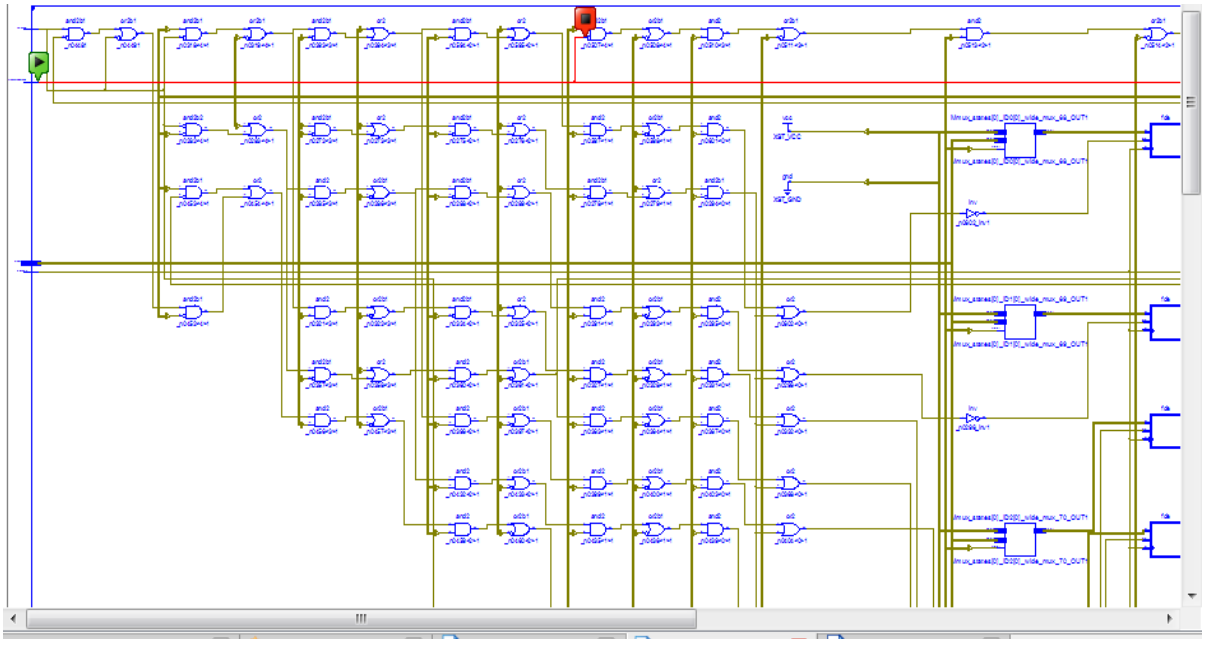

Figure 9. Top left part of the RTL schematic of the storage unit

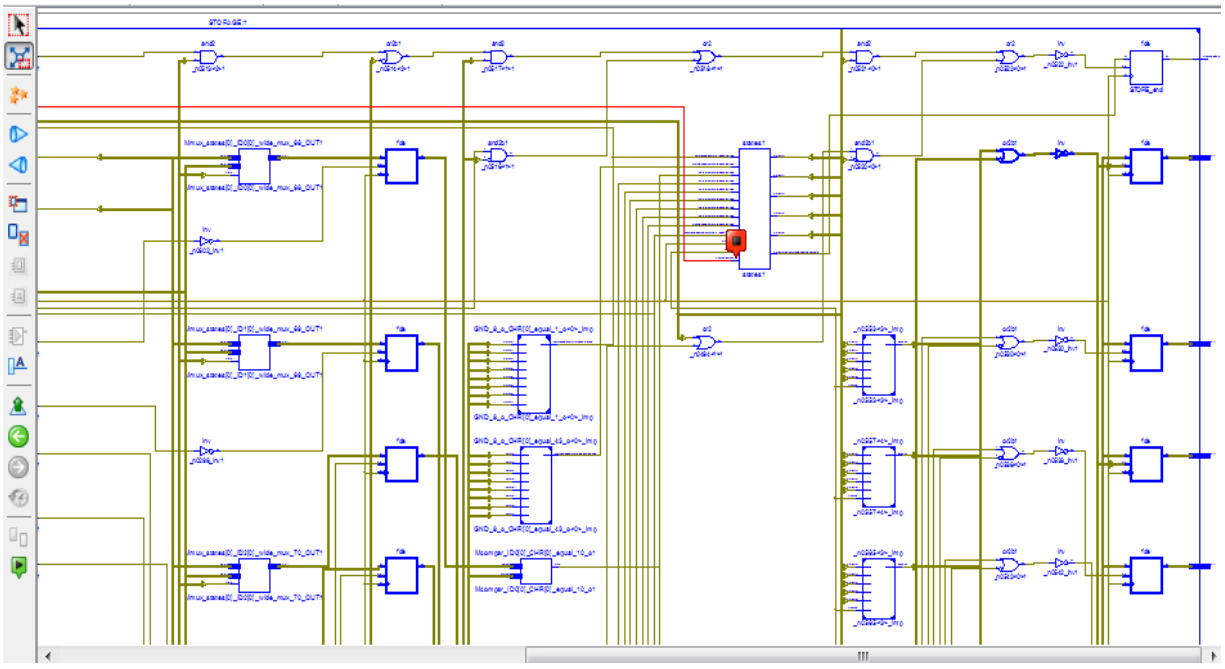

Figure 10. Top right part of the RTL schematic of the storage unit

3. Simulation Results And Design Summary

In this section we are going to show the simulation results for the four main components of the system board (TMU, HMU, ROM, and CU). Where the TMU and HMU are shown in Fig. 11 and 12, and ROM and CU are shown in Fig. 13 and 14 respectively [27]. In Fig. 11 dark, rain, and temp are inputs, and fan, light, roof status, roof forward, and roof reveres are outputs which are controlled according to the status of the input sensors. In Fig. 12, plot sensor represents the input from the humidity sensor after it has been converted using ADC, if the humidity >= 60%, then the output show plot will be '0' as shown in Fig. 12, otherwise it will be 1. In Fig. 13, the simulation results for a 16*8 ROM is shown in which the stored data represent the ASCII code the decimal number (0, 1, 2, …, and 9) and the rest of the locations contain the alphabetic (A, B, C, D, E, and F). Fig. 14 show the simulation results for the CU when sending the AT command "AT+CMGD=1", which means of reading message in location 1. Fig. (14-16) show the simulation results for the control Unit, the UART Transmitter, and UART Receiver [19]. Fig. 14 shows the simulation for the Control Unit which sends parallel data to UART Transmitter; the parallel data represents the ASII code for the characters; the character could be a message or an AT commands. The example given in Fig. 14 is for sending the AT commands for reading message in location 1 "AT+CMGD=1", '$' and '#' are used for the start and end of the transmitted data.

In the simulation we show the transmitted data in the form of characters but in hardware implementation it is stream of bits that represent the ASCII codes of the characters. In Fig. 15, the UART Transmitter is shown in which there are two state, the first one is for preparing data in a frame of 10-bits including the start and stop bits, and the next state is for sending the frame to the serial output S_out, where k is a counter for the number of bits to be send in the second state, and Tx_req and Tx_ready for handshaking. In Fig. 16, the UART receiver is shown, where reg_GSM is a shift register, the input serial data from S_in is shifted in reg_GSM after receiving the start bit, and when rx_en is high, after shifting the 8-bits of the received character and the stop bit, the ASCII character in reg_GSM has to be assigned to P_out.

Figure 11. Simulation results for the temperature effects in the normal operation

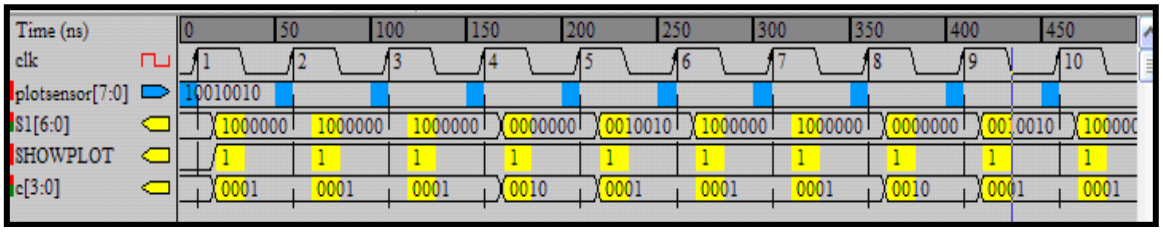

Figure 12. Water level simulation with humidity >= 60% (Normal Humidity)

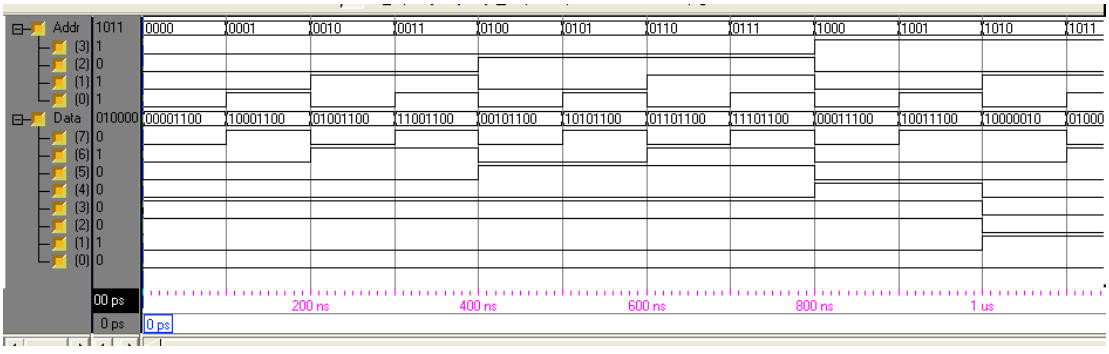

Figure 13. Simulation results for the 16*8 ROM

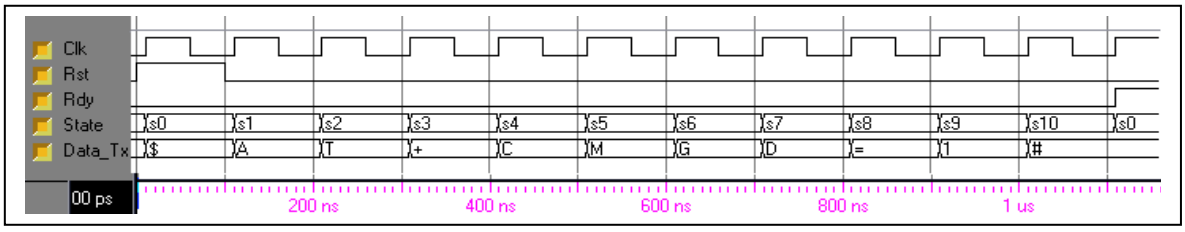

Figure 14. Simulation Results for the Control Unit when sending AT Commands

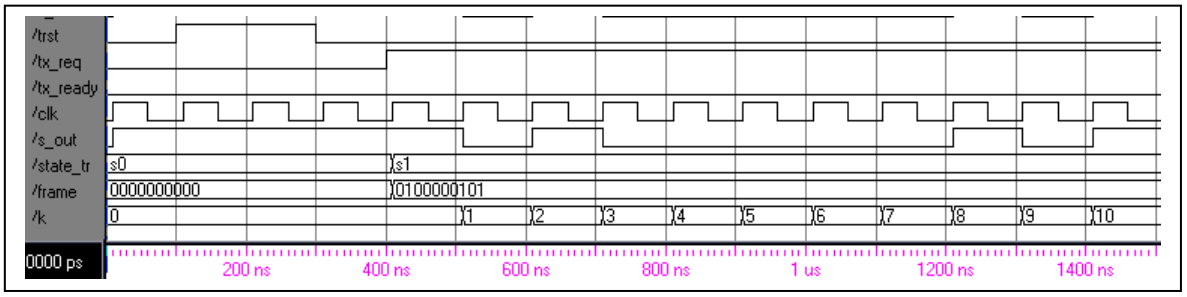

Figure 15. Simulation Results for URAT Transmitter

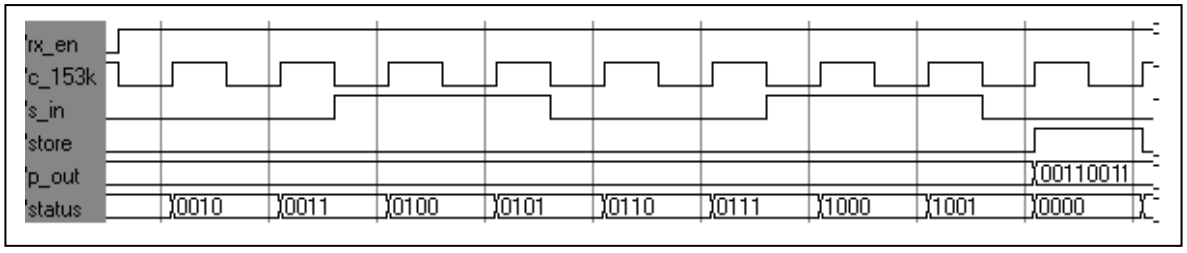

Figure 16 Simulation Results for UART Receiver

Fig. 17 shows the FPGA chip view for the GSM unit generated from Xilinx ISE tools after the implementation process. In Fig. 18 the pin assignment for the design is given using the FPGA xc7vx485t-2ffg1761 device. The design summary and utilized devices is given in table I, where the number of used slice registers is 289 out of 607, 200 (the available slice registers), which indicates that the utilization percentage is 1% for the simple example given in the number of sensing devices. The most consumed devices are the number with an unused Flip Flop (56%), the number of fully used LUT-FF pairs (29%), and the number with an unused LUT (14%). All other devices has a utilization of 1%, 4&, and 6%.

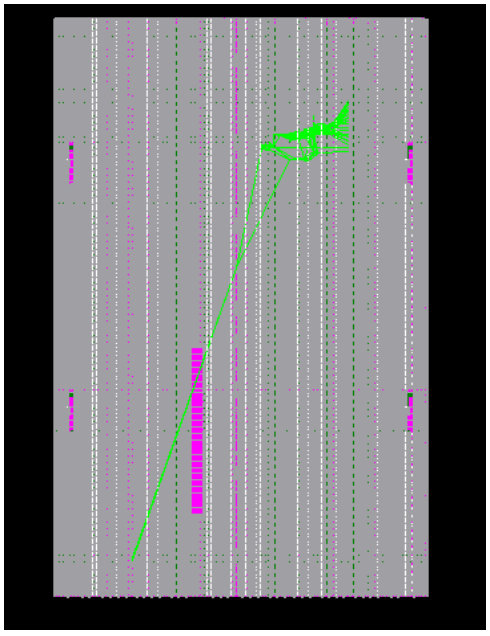

Figure 17 FPGA Chip View for the GSM Unit

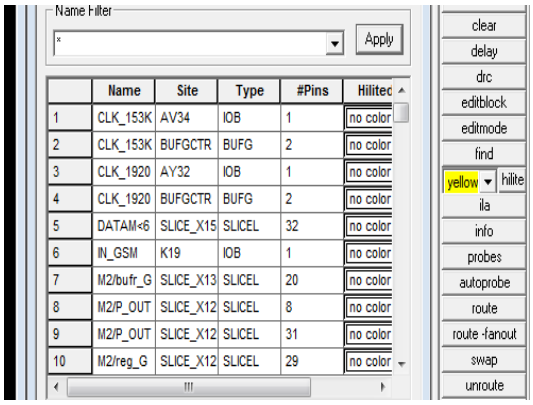

Figure 18 Pins Assignment for the FPGA Chip

Table I. Device Utilization Summary

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	289	607,200	1%
Number of Slice LUTs	513	303,600	1%
Number used as logic	498	303,600	1%
Number of occupied Slices	213	75,900	1%
Number with an unused Flip Flop	339	599	56%
Number with an unused LUT	86	599	14%
Number of fully used LUT-FF pairs	174	599	29%
Number of slice register sites lost to control set restrictions	55	607,200	1%
Number of bonded IOBs	30	700	4%
Number of RAMB36E1/FIFO36E1s	0	1,030	0%
Number of RAMB18E1/FIFO18E1s	0	2,060	0%
Number of BUFG/BUFGCTRLs	2	32	6%
Average Fanout of Non-Clock Nets	3.88		

4. CONCLUSIONS

An FPGA hardware design implementation for IoT based on using GSM has been introduced in this article. The system was designed using VHDL in a high level design method. All parts of the design have been simulated and implemented using Xilinx ISE design suite 14.7. The design has been implemented on Virtex-7 FPGA VC707 Evaluation platform targeting "xc7vx485t-2ffg1761" device with 1761 input/output pins and 200K logic gates. The system was tested in both simulation level using Xilinx tools and hardware level using Digilent Spartan 3 development board. The system still needs some development for final prototype, one of these developments is to use CoolRunner-2 CPLD as the target technology for the hardware implemented. Second is to use GPRS (General Packet Radio Service) for remote monitoring instead of using GSM, to make the design a web-based design that will reduce the cost of usage by avoiding the use of SMS messages in case of GSM.

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