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Novel Ultra Low Power-Delay-Product Full Adder Cells in 45nm Fin-FET Technology

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Abstract: A full adder is one of the most commonly used circuit component, many improvements have been made to refine the architecture of a full adder. The general goal of our work is to reduce power-delay-product (PDP). In this paper two novel 13-transistor CMOS 1-bit Full Adder cell is proposed. The first proposed full adder is based on two stage XOR gate with combined GDI technology and transmission gate. The second proposed full adder uses the low power designs of the XOR and XNOR gates and MUX (2-TR). Our new full adders have been contrasted with following full adders: Conventional CMOS full adder, Complementary Pass Logic, transmission gate adder and transmission function adder. The power and speed has been carried out using extensive simulation on HSPICE circuit simulator. The simulation results are based on 45nm Fin-FET predictive model.

Keywords: *Full Adder cell, GDI technology, Transmission gate, XOR gate, sub-threshold voltage FinFET (sub-FinFET).*

1. Introduction

Addition, multiplication, and multiply then accumulation (MAC) are the fundamental arithmetic operations in the VLSI systems such as microprocessors and digital signal processing (DSP) systems. Most of such arithmetic operations are based on the adder cells. The adder cell not only lies in the critical path, but also consumes the significant power [1-3]. The continual development of recent portable devices and applications has caused an incredible thrust for low power circuit design. Various methods and techniques, such as voltage scaling, clock gating, etc have been applied successfully in the medium power, medium performance region of the design spectrum for lower power consumption [4]. The applications where ultra-low power consumption is the primary requirement and performance is of secondary importance, a more insistent approach is necessary. In the last five years it has been demonstrated that operating the device at minimum energy point (MEP) gives large penalty in delay, whereas minimum energy delay point (MEDP) gives better circuit performance in terms of delay as well as energy and turn out to be the center of attraction for the researchers. However there is a new class of circuit applications which demands for ultra low energy consumption with moderate throughput. These circuits must be operated at minimum energy point to achieve energy at ultra low level. This represents an important mind shift: rather than starting out from a design optimized for maximum performance. The initial design point is now the minimum-energy one. It has been shown that for most of the digital circuit minimum energy point occurs in the sub-threshold operational region of the MOS transistors [5], [6]. However, performance degradation due to minute leakage current as drive current and more sensitivity for process variation due to exponential dependency of drive current on threshold voltage limits its application area. Hence there is pressing need to overcome these limitations by device technology parameter optimization or selecting operating point of the device where both energy and speed are in acceptable range. In this paper, we use the sub-FinFET (sub-threshold voltage Fin-FET) transistors. The new device architecture shows a significant improvement in energy efficiency, delay performance, and also stability to process, temperature, and voltage (PVT) variations while maintaining the almost same ultra low power design constraint.

In this paper, we use the Fin-FET structure to optimize delay, PDP and the robustness for the implementation of full adder cell in sub-threshold region.

In section II is reported double gate devices structure. In Section III explain about some of standard Full Adders. In section IV explain proposed Full Adder

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cells. Simulations and comparisons are developed in Section V. Conclusions are drawn in Section VI.

2. Double-Gate Device

Fin-type field-effect transistors (Fin-FETs) are promising substitutes for bulk CMOS at the nanoscale. Fin-FETs are double-gate devices. The two gates of a Fin-FET can either be shorted for higher performance or independently controlled for reduced transistor count or lower leakage. As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern [2].

The steady miniaturization of metal-oxide-semiconductor field-effect transistors (MOSFETs) with each new generation of CMOS technology has provided us with improved circuit performance and cost per function over several decades. However, continued transistor scaling will not be straightforward in the sub-22 nm regime because of fundamental material and process main challenges in this regime are twofold: (a) minimization of leakage current (sub-threshold þ gate leakage), and (b) reduction in the device-to-device variability to increase yield [11]. Fin-FETs have been proposed as a promising alternative for addressing the challenges posed by continued scaling. Fabrication of Fin-FETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing.

The Fin-FET device consists of a thin silicon body, the thickness of which is denoted by TSi, wrapped by gate electrodes. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer. Due to this reason, the device is termed quasiplanar. The independent control of the front and back gates of the Fin-FET is achieved by etching away the gate electrode at the top of the channel. The effective gate width of a Fin-FET is 2nh, where n is the number of fins and h is the fin height. Thus, wider transistors with higher on-currents are obtained by using multiple fins. The fin pitch (p) is the minimum pitch between adjacent fins allowed by lithography at a particular technology node. Using spacer lithography, p can be made as small as half of the lithography pitches [9]. The architecture of a double-gate Fin-FET with symmetric gates is shown in Fig. 1.

3. Explain about Some of Standard Full-Adders

There are standard implementations with various logic stylesthat have been used in the past to design full adder cells and these are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the outputs, the loads on the inputs and intermediate nodes and the transistor count are varied. Different logic styles tend to favor one performance aspect at the expense of the others. Some of them use one logic style for the whole full adder and others use more than one logic style for their implementation. We call them hybrid logic design style.

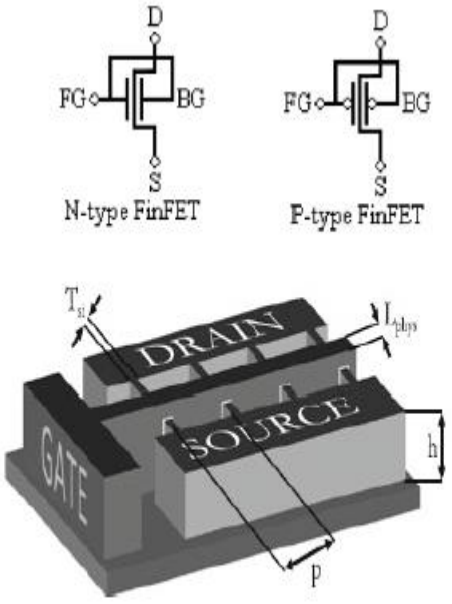

Figure 1. N-type Fin-FET, P-type Fin-FET and symmetrical Fin-FET structure [10].

The complementary CMOS full adder (C-CMOS) as shown in Fig. 2 is based on a regular CMOS structure with conventional pull-up and pull-down transistors and has 28 transistors [11]. C-CMOS generates Cout throughout a single static CMOS gate. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and an NMOS devise. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing. Another conventional adder is the complementary pass-transistor logic (CPL). It provides highspeed,
full-swing operation and good driving capability due to the output static inverters and the fast differential stage of cross-coupled PMOS transistors. But due to the presence of a lot of internal nodes and static inverters, there is large power dissipation. The CPL full adder is shown in Fig. 3 [11].

Another adder is the transmission-gates CMOS adder (TGCMOS) [13], it is based on transmission gates and has 20 transistors), which is shown in Fig. 4. Another adder is the transmission function full adder

cell (TFA), shown in Fig. 5, which is based on the transmission function theory and has 16 transistor [12]. This cell generates the XOR function (H=A XOR B), followed by an inverter to generate the XNOR function ( ). Both H and are used to control the transmission gates generating the Sum and Cout outputs. The inverter introduces unwanted delay between H and leading to a 0-0 or 1-1 overlap. This overlap will cause the transmission gates to act as pass transistors, which may cause glitches (spurious transitions) in the output signals. These glitches will increase the power consumption of these cells.

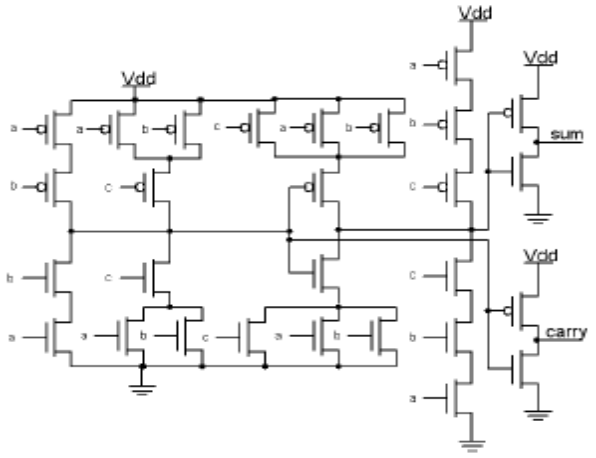

Figure 2. The conventional CMOS adder (CMOS) [11].

4. Proposed Full Adder Cell

4.1. The first 13- transistor Full Adder cell

The proposed Full-Adder is utilized 13 transistors with minimum area. The design of the proposed full adder is based on the design of the XOR gate. The design of a four transistor XOR gate is shown in Fig. 6.

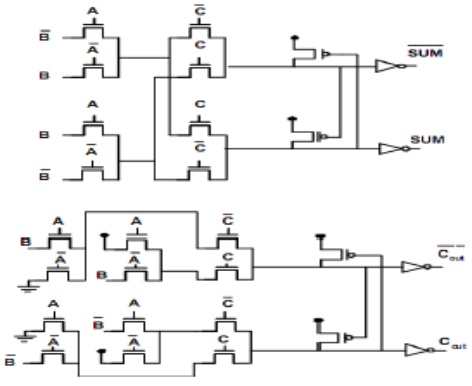

Figure 3. The complementary CMOS logic adder (CPL) [11].

A general method for making sum is to use two stage XOR gate as shown in Fig.7.

In this case, there is a voltage drop problem, which causes the first stage to have static power dissipation. We modify the proposed structure in the first stage with using a pull-up transistor, as shown in Fig. 8. In this state, we have good noise margin and a better high level. Furthermore, the improvement circuit decreases static power dissipation significantly. The size of the pull up transistor is difficult, because if width and length are small there won't be a desired low level. We must be minimizing delay; therefore, the optimization of size of transistors is an effective factor in PDP. Also, there will be glitch in the cascade stage, that we can reduce the glitch effect with the suitable (W/L) ratio of second stage transistor.

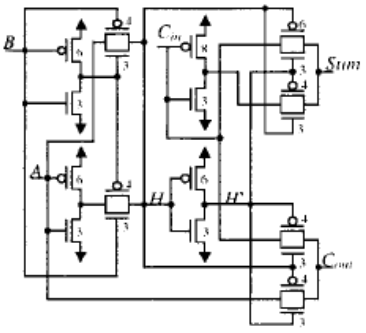

Figure 4. The transmission-gates CMOS adder (TG_CMOS)[2].

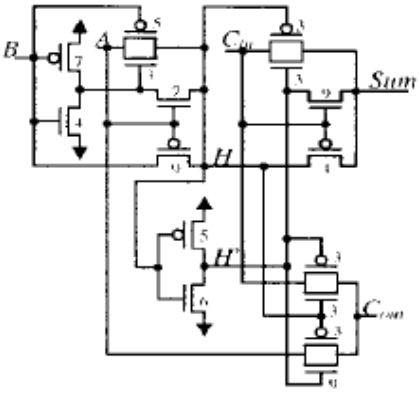

Figure 5. The transmission function adder (TFA) [8].

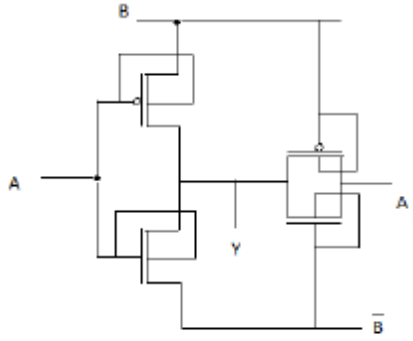

Figure 6. The proposed XOR gate.

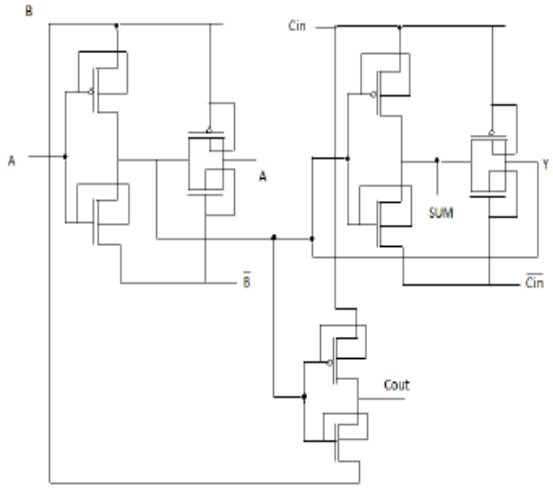

Figure 7. The first proposed Full adder cell

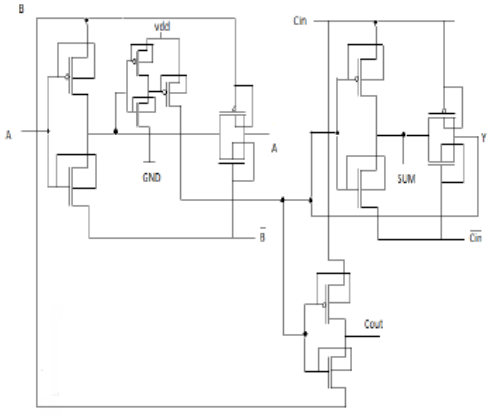

Figure 8. The first proposed Full adder cell

4.2 4.2 The second 13- transistor Full Adder cell

The second proposed adder cell has 13 transistors as illustrated in Figure.6. The transistor number in our new design is the fewest one (TFA has only 16 transistors), also there are fewer glitches existing in our new design as compared with the 16- transistor TFA because XOR and XNOR gates are generated simultaneously. Due to fewer glitches in proposed design, the power can be saved and it has a superior speed enhancement at the same time.

The number of inverters in our new cell is only one, which saves one inverter as the switching activity in our design is lower and the direct path from supply voltage to ground is less. As a result, both dynamic power and short-circuit power can be reduced; and the speed can be increased since the inverter in the critical path has been removed. The proposed new cell has a minimal power-delay product (PDP).

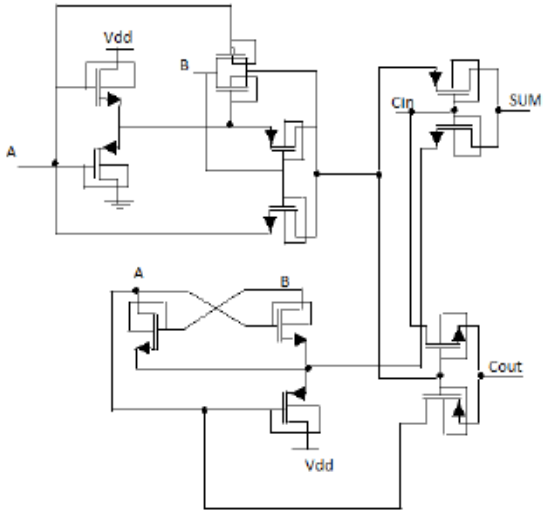

Figure 9. The second proposed Full adder cell

5. Simulation and Comparison

In this section, the proposed Full Adder is evaluated and compared to the other ones. The simulations were done for all four Full-Adders and our design in the same condition. All the results are obtained in 45nm Fin-FET technology with a 0.2V supply voltage. The simulation results are shown in Fig. 10, Fig. 11 and Fig. 12.

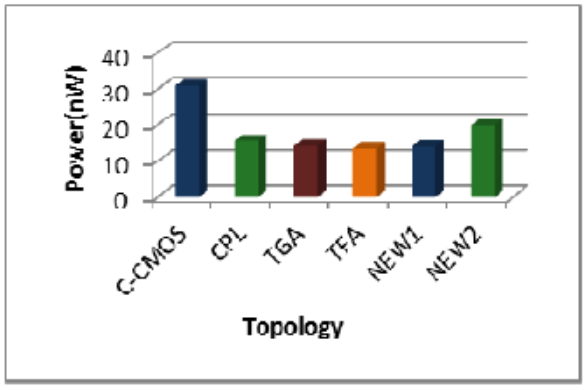

Figure 10. Comparison of power between Fin-FET-based full adder topologies at supply voltage of V_{DD} = 0.20 V

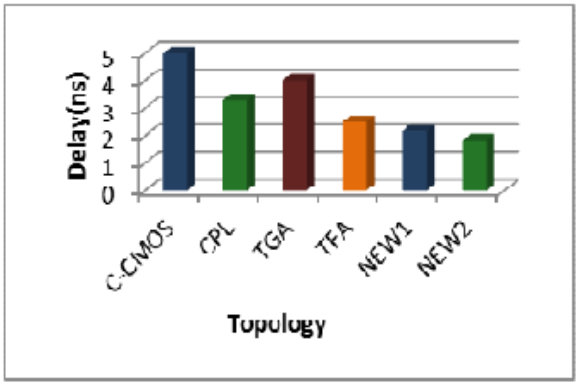

Figure 11. Comparison of delay between Fin-FET-based full adder topologies

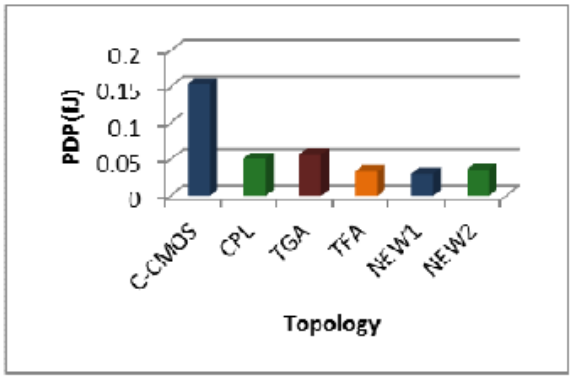

Figure 12. Comparison of PDP between Fin-FET-based full adder topologies at supply voltage of V_{DD}= 0.20 V

6. Conclusion

In this paper, we have proposed two new designs for CMOS 1-bit full adder cell. The proposed circuits are suitable for VLSI applications with low power consumption, small delay, ultra power-delay-product and miniaturized area due to lower transistor counts and specific structures. HSPISE simulation results against four different full adders, which were done at 0.2v supply voltage, shows a significant improvement in PDP.

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