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Design of Two High Performance 1-Bit CMOS Full Adder Cells

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Abstract: 1-bit full adder is a very great part in the design of application particular integrated circuits. Power consumption is one of the most significant parameters of full adders. Therefore reducing power consumption in full adders is very important in low power circuits. In this paper, we propose two new structures of hybrid full adders. The first full adder implemented by combining the Swing Restored Lass-transistor Logic and Branch-Based Logic that called, SRPL-BBL cell and the second full adder implemented by combining the Gate-Diffusion Input technique and Majority function that called, GDI-Majority cell. All of the capacitors in this paper replaced with MOSCAP. Simulation results performed by HSPICE in TSMC 0.13 μm CMOS process. The results indicate the superiority the proposed full adders against several low power 1-bit full adder cells in terms of delay, power consumption, and power delay product (PDP).

Keywords: 1-bit full adder; Low power; SRPL; BBL; GDI

I. INTRODUCTION

Most of the very large scale integration applications, such as digital signal processing, image and video processing, and microprocessors, common use calculation operations. Also, subtraction, and multiplication are examples of the most commonly used operations. The 1-bit full adder cell is the building block of all these modules. Therefore, improvement its performance is acute for enhancing the overall module efficiency.

In addition building low-power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn't advance at the same rate as the microelectronics technology. There is a limited amount of power available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So building low-power, high-performance adder cells is of great interest [1].

1-bit full adder which has three 1-bit inputs (*A*, *B* and C_{in}) and two 1-bit outputs (*Sum* and C_{out}). The relations between the inputs and the outputs are expressed as:

$$Sum = (A \oplus B) \oplus C_{in} \quad (1)$$

$$C_{out} = A.B + C_{in}.(A \oplus B) \quad (2)$$

There are many logic styles for design digital circuits which a main influences the circuit performance. A gate is evaluated by three basic parameters, area, delay time (propagation delay) and power consumption. Depending on the application, the emphasis will be on different parameters.

The delay time depends on the size and number of transistors, the parasitic capacitance including intrinsic capacitance and capacitance due to routing and the number of logic gates. The power consumption depends on the switching activity, size and number of transistors, glitch, leakage current of transistors and sub-threshold current [2], [3].

Power consumption in CMOS digital circuits is divided into three main parts as follows [4]:

$$P_{Total} = P_{Dynamic} + P_{Short-circuit} + P_{Static} \quad (3)$$

Due to Charging and Discharging Capacitances.

Due to the current between power supply and ground during a

transistor switching. Due to the leakage current and static current [2], [5].

There are many papers in the field of low power full adder design. In [6] a hybrid full adder by combining complementary pass-transistor logic (CPL) and transmission gate logic (TG) is proposed. In [7], a 14-transistor 1-bit full adder cell is proposed. In [1], ULP full adder (ULPFA) is proposed. In [8], [9] high speed 1-bit fast full adder cell using the GDI technique is proposed.

In this paper we will present two low power CMOS 1-bit adder cells. The paper is organized as follows. In Section II we will study the branch-based logic (BBL) style, swing restored pass-transistor logic (SRPL) style, gate-diffusion input (GDI) and majority function. In section III the proposed full adders are presented. Simulation results in Section IV and conclusion in Section V is expressed.

II. Survey of SRPL, BBL, Gate-Diffusion Input and Majority Function

A. SRPL Style

The general SRPL gate includes two basic parts as shown in Fig. 1. Complimentary output pass-transistor logic network that is constructed of n-channel devices and a latch type swing restoring circuit consisting of two cross-coupled CMOS NOT gates. The gate inputs are of two kinds:

1) *Pass variables that are connected to the drains of the logic network transistors.*
2) *Control variables that are connected to the gates of the transistors.*

The logic network has the ability to implement any Boolean logic function [10].

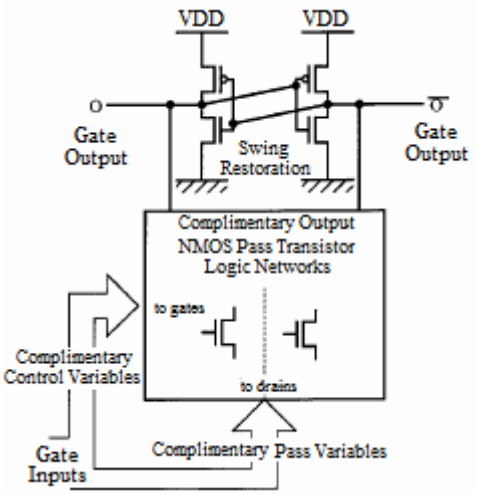

Figure 1. General SRPL gate [10].

B. BBL Style

A logical function can always be delineated with only branches [2]. In BBL style, logic cells are designed only with branches composed of transistors in series connected between a power supply and the gate output. The two major advantages of this style are implement a more compact design and reduce power consumption.

For example, the symbolic layout of the non-branch-based P-channel network (Fig. 2 (a)) includes two supplementary contacts with two drain parasitic capacitances that can be removed in the more compact branch-based implementation (Fig. 2 (b)). The symbolic layout of Fig. 2 comes from the following logical equation [11]:

$$S = (B + C).(A\bar{C} + \bar{A}D) \quad (4)$$

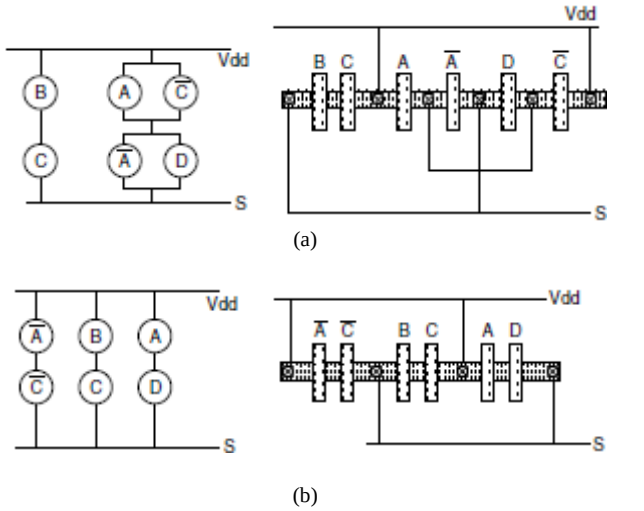

Figure 2. Diagram and layout of the logic cell, (a) Without the use of BBL style, (b) With the use of BBL style [11].

C. Gate-Diffusion Input

Gate-Diffusion Input (GDI) is proposed by Morgenshtein [12]. It is a wizard design which is very flexible for digital circuits. Moreover, it is power efficient without massive amount of transistor unit. The main problem of a GDI cell is that it requires twin-well CMOS or silicon on insulator (SOI) process to actualize [13]. The Gate-Diffusion-Input technique is based on the use of a simple cell as shown in Fig. 3. The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). Bodies of both NMOS and PMOS are connected to N or P respectively [8].

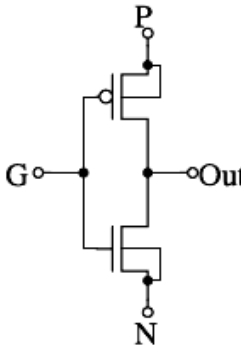

Figure 3. Basic Gate-Diffusion-Input cell [13].

Multiple-input gates can be performed by combining several GDI cells. The truth table of functions is shown in Table I.

TABLE I. FUNCTIONS OF THE BASIC GDI CELL

Input			Out	Function
P	G	N		
B	A	0	$\bar{A}.B$	F_1
1	A	B	$\bar{A}+B$	F_2
B	A	1	$A+B$	OR
0	A	B	$A.B$	AND
B	A	C	$\bar{A}.B+A.C$	MUX
1	A	0	$\bar{A}$	NOT

D. *Majority Function*

The majority gate is created with input capacitors and a static CMOS inverter. A 3-input Majority Not gate implemented with this method is illustrated in Fig. 4. We can also design majority gates with more inputs by this method by increasing the number of input capacitors. The capacitor network is used to provide voltage division for implementing majority logic. When the majority of inputs are "0", the output of the capacitor network is considered as "0" by the inverter and consequently the output of inverter is . When the majority of inputs are "1", the output of capacitor network is considered "1" by the inverter and consequently the output of inverter is 0. The input capacitance of the inverter is measured as about 0.05 fF, which is negligible and has no effect on the operation of the circuit

The capacitors network divide the voltage level of three inputs (*A*, *B* and) and then , the following CMOS inverter corrects the voltage level to if the divided voltage becomes higher than 1/2 , and to GND if it becomes lower than 1/2 [14].

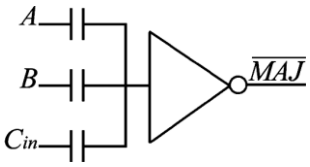

Figure 4. Majority Not gate [14]..

III. PROPOSED 1-BIT FULL ADDER CELLS

In this section we proposed two new full adders. The *Sum* block and C_{out} block of the first full adder that called SRPL-BBL is designed using SRPL style and BBL style respectively. Also the *Sum* block and C_{out} block of the second full adder that called GDI-Majority is designed using GDI technique and Majority function respectively. The advantages of these full adders are: low power, low delay and low PDP.

A. *GDI-Majority*

Transistor level schematic of the first proposed full adder is shown in Fig. 5. These full adders robustness against voltage scaling and transistor sizing enables it to operate reliably at low voltage.

The truth table of the first full adder (Fig. 5) is shown in Table II.

TABLE II. TRUTH TABLE OF THE FIRST FULL ADDER

A	B	C_{in}	C_{out}	sum	Majority function
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	1	1

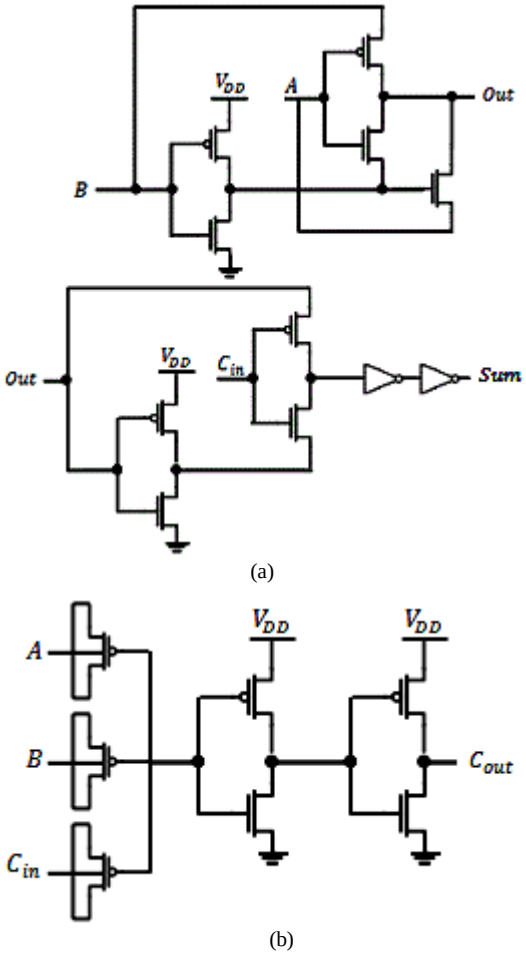

Figure 5. Schematic of the first proposed full adder cell, (a) *Sum* block, (b) block.

The optimize size of MOSCAPs that we used in this paper are L=0.18µm, W=0.75µm. Mathematical equations for proposed full adder are:

$$Sum = (A \oplus B) \oplus C_{in} \quad (5)$$

$$C_{out} = Maj(A, B, C_{in}) \quad (6)$$

$$Maj(A, B, C_{in}) = A.B + A.C_{in} + B.C_{in} \quad (7)$$

New full adder is optimized and tested separately in various voltages.

B. SRPL-BBL

Transistor level schematic of the second proposed full adder is shown in Fig. 6. The obtained equations for the NMOS and PMOS networks of C_{out} are expressed as [2]:

$$C_{out,NMOS} = \bar{A}.\bar{B} + \bar{A}.\overline{C_{in}} + \bar{B}.\overline{C_{in}} \quad (8)$$

$$C_{out,PMOS} = \bar{A}.\bar{B} + \bar{A}.\overline{C_{in}} + \bar{B}.\overline{C_{in}} \quad (9)$$

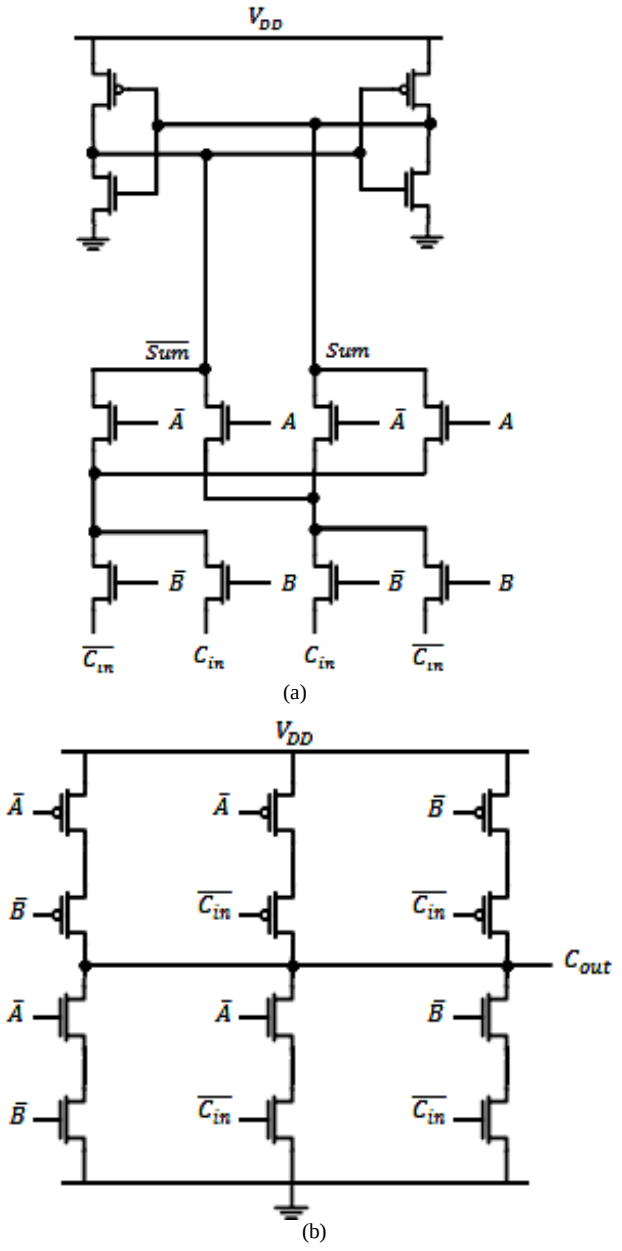

Figure 6. Schematic of the second proposed full adder cell, (a) *Sum* block, (b) block.

Value of C_{out} for different inputs is shown in Table III.

TABLE III. VALUES OF

$\bar{A}$	$\bar{B}$	$\overline{C_{in}}$	C_{out}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

.

IV. SIMULATION RESULTS

Simulation results are performed by HSPICE in TSMC 0.13 µm CMOS process with the 1.2 V supply voltage, 12.5 MHz operating frequency and 25 ℃ temperatures. The snapshot of the waveforms at 1.2 V is shown in Fig. 7.

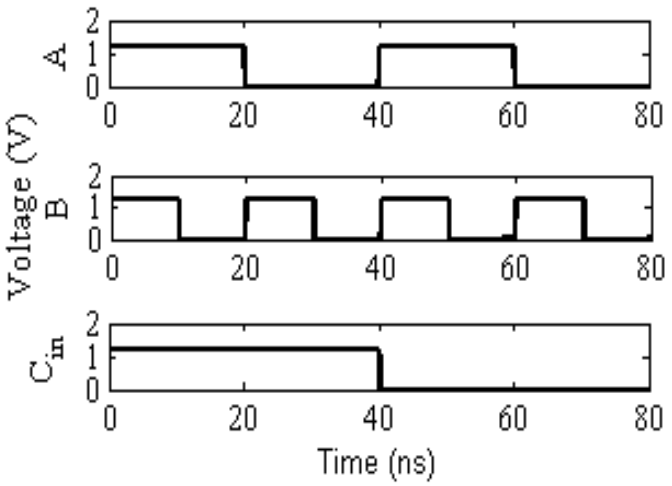

Figure 7. Snapshots of waveforms at 1.2V and 12.5MHz.

Simulation results for first and second proposed full adder are shown in Fig. 8.

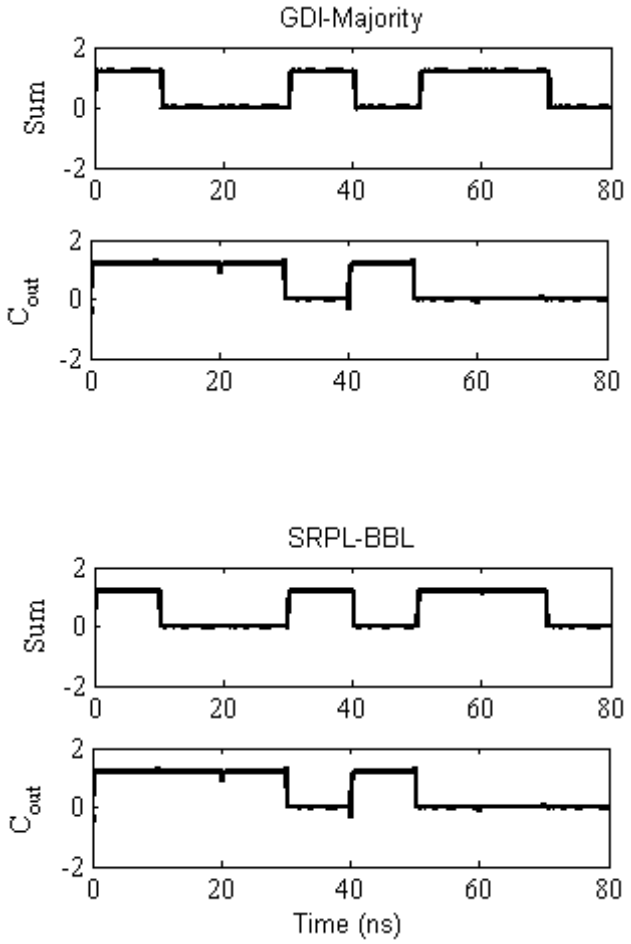

Figure 8. The output waveforms of proposed full adders

All the possible input transitions are tested to correct results. The delay parameter is calculated from the time that the input reaches 50% of the power supply level, to the time that the output reaches the same voltage .rising and falling propagation delay are separately measured for both *Sum* and . The maximum delay of all the transitions is taken as the cell delay. The results for delay, power consumption and PDP parameters are separately illustrated in Fig. 9, Fig. 10 and Fig. 11 respectively.

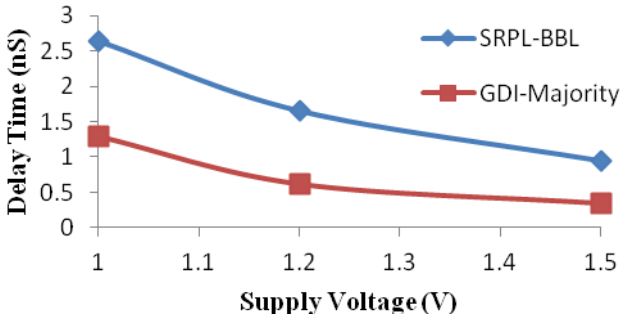

Figure 9. Delay of the full adder cells, versus supply voltage.

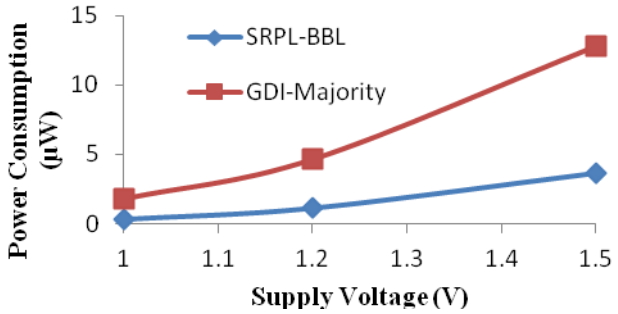

Figure 10. Power consumption of the full adder cells, versus supply voltage.

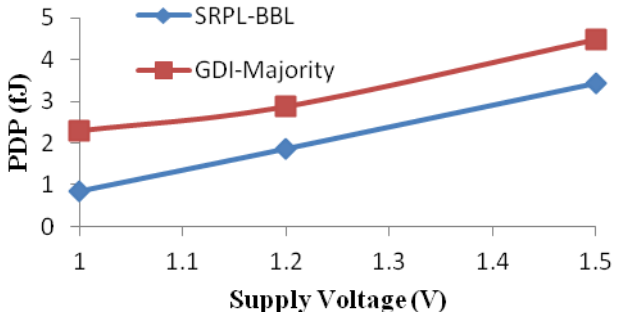

Figure 11. PDP of the full adder cells, versus supply voltage.

In Table IV, the results of the proposed full adder are compared with some low power CMOS full adders. Also for a fair comparison, all full Adders presented in Table IV, again simulated by HSPICE in TSMC 0.18 µm CMOS process with the 1.2 V supply voltage, 12.5 MHz operating frequency and 25 ℃ temperatures.

V. CONCLUSION

Two novel designs according to the SRPL, BBL, and GDI technique and majority function for 1-bit CMOS full adder cells are presented. The characteristics of the proposed full adders are compared against previous designed full adders based on the worst case delay time, power consumption and power delay product.

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TABLE VI. SIMULATION RESULTS FOR 1.2 V AND 12.5 MHZ

	Full Adder	***Power Consumption (µW)***	***Delay (ns)***	***PDP (fJ)***	***Device Count***
	Conventional Static CMOS [3]	8.230	0.356	2.930	28
	CPL [2]	10.02	0.260	2.605	32
	BBL-PT [2]	7.980	0.320	2.554	23
	Bridge [15]	6.360	0.318	2.020	32
Proposed	***GDI-Majority***	4.620	0.622	2.870	20
	SRPL-BBL	1.130	1.650	1.8650	24