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Exploring the Effect of Switch ON Resistance on the Performance of Various Class E Power Amplifier Topologies

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Abstract: Although the working of class E Power Amplifiers (PA) based on various tuned circuits is very well presented in the referenced papers, the performance disparities due to non-idealities in switching device is not very well discussed. Moreover, there is a lack of comparative study of the same with respect to diverse class E PA topologies. Capturing the effect of parasitics of the switch correctly plays an important role in the PA design, as the design equations with parasitics are greatly affected. This paper aims to explore the impact of the saturation/ON resistance of the switching device on power amplifier performance parameters. The paper presents the analysis and comparison of various SMPA topologies based on the diverse tuned circuit networks. The analysis is done at 2.4 GHz Industrial, Scientific and Medical band (ISM). It is observed that with the variation of switch resistance in the ON state, the power added efficiency and the power delivered to the load indicates an inverse dependence. Furthermore, as the saturation resistance increases more harmonics are observed at the load which in turn increases total harmonic distortion. The power loss in the switching device is also investigated and is found to have a direct relationship with the switch ON resistance.

Keywords: Switched Mode Power Amplifiers, ISM band, Power Added Efficiency, Total Harmonic Distortion

1. INTRODUCTION

The power amplifier (PA) being the main source of power loss in the transmitter of a wireless communication system has become a prime research interest for PA designers. [1]. A designer has to make several suitable trade-offs to make the PA fit for a certain application. PA design depends mainly on the operating frequency, the device technology available and the area of its usage [2], [3]. Power amplifiers are mainly grouped as linear and switched-mode amplifiers. Linear amplifiers comprise of class A, B, AB and C power amplifiers [4]. These are defined by the length of the cycle for which the current of the output stage transistor flows through the load. Linear power amplifiers are called so because the output of the amplifiers is a linear function of the amplifier input [5] [6]. The other class, namely switched-mode power amplifiers (SMPAs) are called so because the transistor is driven as a switch. This improves the PA efficiency considerably, but at the same time, the shape of the signal is not preserved. As such, SMPAs are non- linear in nature [7]. Class D, E and F are the classic examples of switched-mode power amplifiers [8] [9] [10]. SMPA becomes a good choice for battery critical applications that require high efficiency. Among the various classes of SMPA, the class E amplifier is the most area-efficient in addition to being highly power efficient as will be discussed in the rest of the paper. Hence, it becomes best suited for biomedical applications at the ISM band.

Class E PA has been extensively studied since it was first introduced by Ewing in 1965 and later by Sokal in 1975 [10] [11]. Researchers have proposed numerous variations in class E PA, thus catering to a large number of applications. Generally, the basic assumption made in the design of the class E PA is that the switching device has an ON resistance (R_{ON}) equal to zero ohms. This condition, although possible ideally, has no practical significance. A switching device like BJT, MOSFET, etc., has inherently a finite value of saturation resistance that has a high impact on the performance parameters of the power amplifier [12] [13]. The resistance is itself inherently dependent on many physical and metallurgical parameters of the substrate used to design the switch, which leads to its non-ideal operation thereby resulting in many disparities. The authors in most of the existing work have assumed idealistic assumptions in designing the PA and no proper work that considers disparity due to switch saturation resistance has been reported yet. Capturing the effect of parasitics of the switch correctly plays an important role in the PA design, as the design equations of PA with parasitics are greatly affected.

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In this paper, therefore, the effect of the finite value of saturation resistance of the switching device on power added efficiency (PAE), power output (P_{load}) and total harmonic distortion (THD) of various class E switched-mode amplifier topologies have been studied. The experimental analysis is carried out initially using an ideal switch from general design kit (GDK) library followed by 0.12 µm RF MOS transistor from United Microelectronics Corporation (UMC) foundry. Results using both the device are comprehensively analyzed and discussed. It is observed that the PAE and P_{load} both depend inversely while THD has a direct dependence on the switch ON resistance. The power loss due to finite ON resistance has also been studied which increases with the increase in ON resistance.

The rest of the paper is organized as follows. Section 2 presents a concise discussion about switch-mode power amplifiers. The operational detail of the class E amplifier is given in section 3. Section 4 discusses the diverse topologies of class E PA in detail. Section 5 gives insight into the results obtained presents a comprehensive analysis of the same. Finally, the conclusion of this work is discussed in section 5.

2. SWITCHED MODE POWER AMPLIFIERS

In switched-mode power amplifiers, the transistor operates as a switch, i.e. either in saturation or in cut-off mode. Power dissipation in a circuit is defined as the product of voltage and current in the circuit, integrated and averaged over the time period. Thus, in order to decrease the power dissipation in the circuit, the voltage and current must not exist simultaneously in the system. The transistor must withstand high voltage and conduct high current for some part of the signal. But, if the circuit is organized in such a way that higher currents and voltages do not overlap, then the power dissipation can be appreciably decreased. This is the basic idea behind the operation of SMPA [14], [15]. This implies that the voltage and current waveforms of the transistor should look like Fig. 1 and hence the theoretical efficiency of 100% can be achieved [16]. But, practically, the efficiency is restricted, as the transistor never behaves as an ideal switch causing the V-I waveforms to overlap. The transistor in an SMPA is usually driven by a square wave to make it work as a switch. Therefore, the PA output is made up of various odd harmonics which needs to be filtered out to retrieve the fundamental harmonic at the output. This is done by choosing a proper load network that consequently decides the class of SMPA [17] [18]. SMPA performance is primarily assessed by the output power it can deliver and its power-added efficiency. In this paper, these two metrics along with the total harmonic distortion at the output of the power amplifier are investigated. The output power of the PA is defined as the total power delivered to the load within the desired range of frequency. The power gain is given by the ratio of output power (P_{load}) to the input power

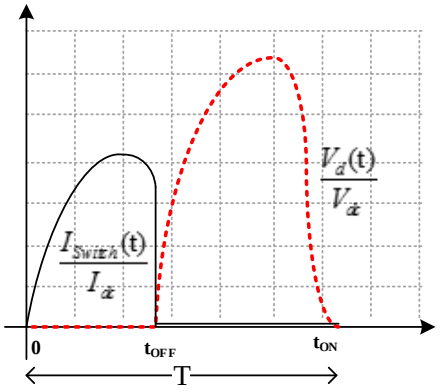

Figure 1. The theoretical waveform of Class E SMPA

(P_{in}). Power amplifier efficiency indicates how efficiently the DC supply power is converted into useful RF power delivered to the load The PAE is one of the commonly used definitions for PA efficiency and is defined as:

$$PAE(\%) = \frac{P_{load} - P_{in}}{P_{dc}} \times 100 \quad (1)$$

Where P_{dc} is the total DC power drawn from the voltage supply [19][20]. Total harmonic distortion measures the amount of energy in the harmonics, compared to the energy in the fundamental harmonic [21] [22]. It can be defined as the ratio of the square root of the sum of squares of the amplitudes of all the harmonics to the amplitude of the fundamental harmonic Where a_n is the amplitude of n^{th} harmonic at the output.

$$THD = \frac{\sqrt{a_1^2 + a_2^2 + a_3^2 + ...a_n^2}}{a_1} \quad (2)$$

3. CLASS E PA OPERATIONAL DETAILS

Class E switched-mode amplifier circuit comprises an active device driven to operate as a switch with a parallel capacitance, a load network made of reactive elements, and a load resistor. The parasitic capacitance of the device and the stray capacitance of the circuit can be incorporated into the design through this shunt capacitance. For the amplifier to work in class E mode, certain conditions need to be fulfilled as mentioned below [23][24]:

i). The voltage across the switch is driven to zero before turn ON i.e. at the end of OFF state i.e.

$$V_{Switch}(t)\big|_{t=t_{ON}} = 0 \quad (3)$$

This is called Zero Voltage Switching (ZVS). It ensures the elimination of discharge losses during this transition.

ii). $$\left.\frac{dV_{Switch}(t)}{dt}\right|_{t=t_{ON}} = 0 \quad (4)$$

This ensures the current through the switch at the commencement of the ON state is zero. This is called Zero Voltage Derivative Switching (ZVDS).

iii). When the switch turns OFF, the build-up of voltage across it is delayed until the current from the previous ON state has reduced to zero. This is achieved by the presence of a capacitor in parallel with the switch.

The basic circuit of a class E amplifier is given in Fig. 2. When the switch is closed, a DC offset sinusoidal current flows from resonator into the switch. When the switch is open, the resonator draws the current back from the switch through the shunt capacitor which acts as a return path. Hence, the sinusoidal current alternates between the switch and the capacitor. The resonator is tuned at the frequency of interest, blocking the harmonic frequencies and DC. This ensures that the output current is a pure sinusoid [25] [26]. This is the idealized operation of a class E PA with the following assumptions:

a) The transistor acts as an ideal switch with zero ON resistance and zero saturation voltage.
b) The duty cycle of the waveform is 50% which is optimum for class E operation.
c) RF choke is ideal.
d) Lumped components do not contain any parasitics.
e) The quality factor of the resonant network is infinite.

The class E PA can achieve 100% efficiency under these assumptions. In this paper, all these assumptions are considered except that the ON resistance of the switch is taken as non-zero. The demerit of Class E PA is that the voltage and current swings can be very high, pushing the reliability of the device [27] [28]. The class E PA has definite design equations, which are specific for the tuned circuit network used in that PA. These design equations provide guidelines for the designer to conceive an application-specific PA [29] [30].

The researchers have made numerous modifications to the basic class E PA topology, especially to its tuned circuit. This has yielded a large number of class E PA variants, each good for some specific application. In this paper, six different topological variants of class E PA have been studied. These variants are mentioned in Table I.

TABLE I. VARIOUS CLASS E PA VARIANTS

Topology	Type of Tuned Circuit/DC feed
T-I.	Shunt Capacitance series tuned Class E PA.
T-II.	Class E PA with Shunt Inductor
T-III.	Even Harmonic resonant class E PA
T-IV.	Class E PA with finite DC feed inductance
T-V.	Inverse class E PA
T-VI.	Inverse class E PA with finite DC feed inductance

4. TUNED CIRCUIT BASED CLASS E PA CLASSIFICATION

The various class E variants mentioned in Table I are discussed in detail in this section. Fig. 2 gives the classical form of class E PA as given in [31] [32]. A radio frequency choke (RFC) is used that allows only pure DC to flow in the circuit. The shunt capacitor aids in absorbing the device parasitics into the PA design [33]. The resonant network comprises of a series LC circuit tuned at the fundamental frequency. The load resistor in an SMPA is chosen such that it presents the load line match (power match) instead of a conjugate match. In later, the maximum power delivered to the load does not account for full ratings of the transistor i.e. the device will deliver less power than its specified limit. But, in a power match, full utilization of the transistor capacity is ensured. Such a load resistor is called the optimum resistor (R_{opt}) [34]. Being a basic variant, the working of this topology has already been discussed in section 3. The presence of RF choke makes this configuration bulkier as well as lossy [35]. The circuit in Fig. 3 has an inductor in parallel with the device instead of a capacitor [36] [37]. The RFC is omitted in this topology, hence lowering the losses as well as size. When the switch is turned OFF, the current through it drops to zero. Hence, the sinusoidal current that flows through the shunt inductor (L_s) and the load resistor (R_{opt}) is the same. This current produces a voltage drop across L_s. The difference between the supply voltage (V_{dd}) and the voltage across L_s appears across the switch. When the switch is closed, the switch voltage drops to zero making the voltage across L_s equal to V_{dd}. This voltage produces the current through L_1, which increases linearly with time. This design increases the drain efficiency by restricting the power dissipation to ON to OFF transition.

Fig. 4 depicts a modified class E amplifier that eradicates the need for an RF choke by adding an inductor (L_{sh}) and shunt capacitor (C_{sh}) to the switch [38]. The voltage source V_{dd} supplies the current through inductor L_{sh} into the circuit. This current is converted into high-frequency current by the switch. The output load network permits only the fundamental frequency to the load resistor. Due to the transition phenomenon of L_{sh} and C_{sh}, the voltage and current waveforms of the switch becomes smooth, thus minimizing the power losses. Moreover, for this circuit, the purpose of RFC is met by the short inductor L_{sh}. The degree of freedom for designing this circuit is limited. In [39], the topology of Fig. 2 is modified into Fig. 5 wherein the RF choke is replaced by a finite DC feed inductance. This alteration makes it suitable for implementation on-chip. Moreover, in this paper, the author has proposed time-domain analytical equations for the design of class E PA making it less complex. Also, the effect of duty cycle variation and finite DC feed inductance

has been investigated. This topology gives more degrees of freedom to design and optimize the circuit.

The circuit illustrated by Fig. 6 is the dual of class E PA and is called Inverse class E PA [40] [41]. The dual criteria that this class of PA satisfies is given as:

1. $I_{Switch}(t)|_{t=t_{ON}} = 0$. (5)

   This is called Zero Current Switching (ZCS).

2. $\left.\frac{dI_{Switch}(t)}{dt}\right|_{t=t_{ON}} = 0$ (6)

   This is called Zero Current Derivative Switching (ZCDS). This makes the voltage across the switch at this instant zero allowing for slow turn OFF without severe efficiency degradation.

The switching action of the transistor drives a sinusoidal voltage across the load resistor through the parallel resonator L_pC_p. The DC block capacitance (C_x) isolates the supply from the output signal in addition to preventing L_p from shorting the DC supply. The consequences of replacing the series resonator with a parallel tuned network are that the peak current flowing into the resonator inductor is higher, but the peak voltage across the resonator capacitor is lower. Moreover, the peak voltage across the switch is 20% lower than the class E PA.

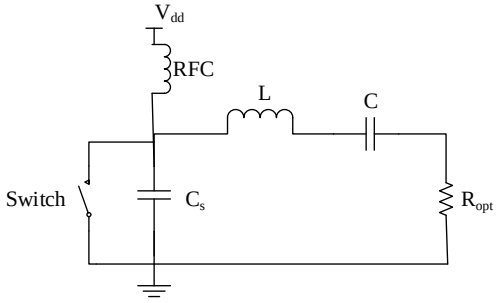

Figure 2. Shunt Capacitance series tuned Class E PA.

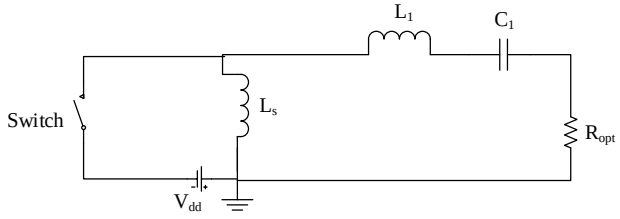

Figure 3. Class E PA with Shunt Inductor

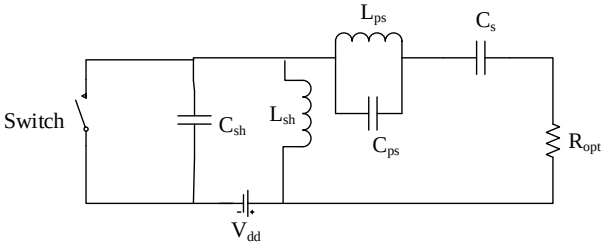

Figure 4. Even Harmonic resonant class E PA

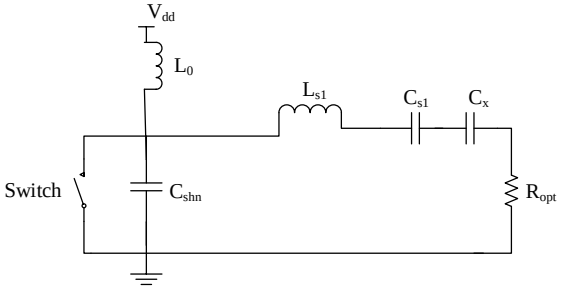

Figure 5. Class E PA with finite DC feed inductance

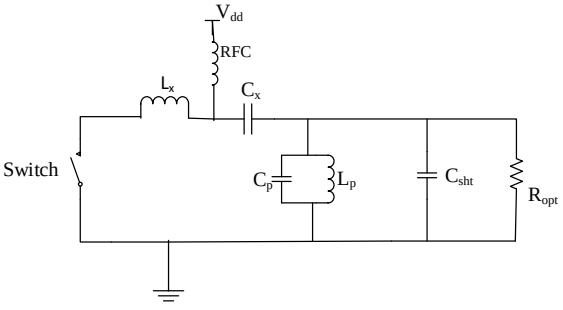

Figure 6. Inverse class E PA

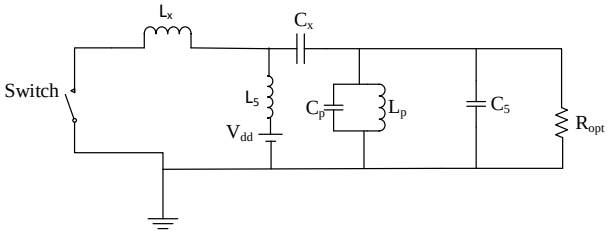

Figure 7. Inverse class E PA with finite DC feed inductance

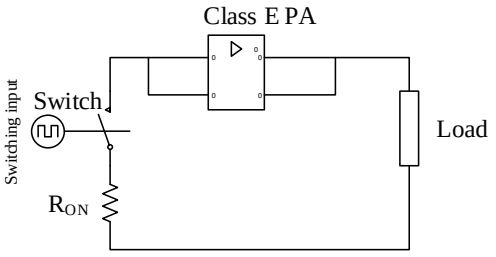

Figure 8. Block of class E PA with the switch ON resistance

Therefore, it can sustain more current through it when ON and handle more voltage across it when OFF, compared to class E PA. Also, in inverse E PA, the parasitic series inductance of the device can be absorbed by L_x, that prevents deterioration of the amplifier operation. But, this dual version of class E PA is less attractive for practical applications, especially at high frequencies. This is because they require a switch with negligible capacitance.

Fig. 7, depicts a modified version of inverse class E PA in which RFC has been replaced by a finite DC feed inductance [42]. This alteration makes it suitable for Monolithic Microwave IC design (MMIC) as it shows appreciable improvements in size, complexity and cost. The various variants of class E PA discussed so far are implemented first using an ideal switch in series with resistance and then using RF MOSFET from UMC for 120 nm technology node at 2.4 GHz. The ON resistance of the switching device is varied and these topologies are compared for their PAE, P_{out}, power loss and Total Harmonic Distortion (THD). The tool used is the Agilent Advanced Design System (ADS). A comprehensive discussion on results is presented in the next section.

5. RESULTS AND ANALYSIS

The Class E topologies as discussed in this paper, have been analysed and compared for various performance metrics namely PAE, Pout and THD. The power dissipated due to the ON switch resistance has also been analyzed.

In the case of low voltage PA design, the overall degradation of PA performance with respect to the finite value of R_{ON} of the switching device needs to be anticipated. Fig. 8 shows the block illustration of class E PA with ON saturation resistance in series with an ideal switch. Due to the limitation of an evaluation algorithm in the tool, the least possible value of ON resistance used is 0.01 Ω. The OFF-state resistance can be set according to the need, 1M Ω for this simulation. With these constraints, Fig. 9 (a) to Fig. 9 (f) correspond to the plots of switch voltages and switch currents at different values of ON resistance for all the six topologies. As can be seen from the figure, the switch voltage increases while the switch current decreases with the increase in R_{ON} in all the six topologies. This implies that during ON state, the switch currents and voltages are both non zero and hence their overlap causes power dissipation in the switch. Therefore, for a finite value of ON resistance, the optimum conditions for ideal class E operation do not correspond to minimum power loss requirements

Table II and III present the values for peak switch voltages and switch currents for all the topologies at different values of ON resistance. It can be inferred from the table that with the increase in channel resistance during ON state, the peak value of voltage across the switch increases while the peak value of current through it decreases. This variation differs from one topology to the other based on how strong is the influence of R_{ON} on a particular circuit.

Fig. 10 illustrates the effect of change in switch voltage with respect to the change in switch ON resistance. If Ψ_i is the value of switch current or switch voltage at the i^{th} sample, then the percent change in Ψ is given by:

$$\Delta\psi = \frac{\psi_{i+1} - \psi_i}{\psi_i} \times 100 \tag{7}$$

Where ΔΨ is the percent change in Ψ. As depicted in Fig. 10, the drastic change in switch voltage in all the circuit topologies occurs when R_{ON} increases from 0.01 Ω to 2.5 Ω. After 2.5 Ω, the change observed has a gradually lesser slope. Moreover, among the six topologies, the maximum impact of R_{ON} variation is observed in topology II (T-II) while the topology I (T-I) gets least affected. For example, in T-I, when R_{ON} changes from 0.01 Ω to 2.5 Ω, the switch voltage increases by approximately 20 times while in T-2 the increase in switch voltage is by 374 times. This is evident from the nature of the circuit where there is no parallel capacitor, but instead, a shunt inductor is placed. Similarly, Fig. 11, shows the variation of switch current with the change in R_{ON}. As expected, the change in switch current follows the trend opposite to that of switch voltage. T-I demonstrates the maximum influence on switch current variation due to R_{ON} change while T-II shows the minimum effect. The switch current in T-I decreases by around 250 times while it decreases by 0.9 times in T-II.

From the discussion above, it is clear that due to the finite value of switch ON resistance, non-zero values of switch voltage do coexist with the switch current during the ON state of the switch. This causes power to be dissipated in the switch during turn ON state. The power loss in the switch due to R_{ON} can be calculated as [5] [43]:

$$P_{loss} = \frac{R_{ON}}{2\Pi} \int_0^{\Pi} {i_{ON}}^2(t)dt \tag{8}$$

For an optimum class E PA with a 50% duty cycle, the power loss is given by [44]:

$$P_{loss} = 1.365 \frac{R_{ON}}{R_{load}} P_{dc} \tag{9}$$

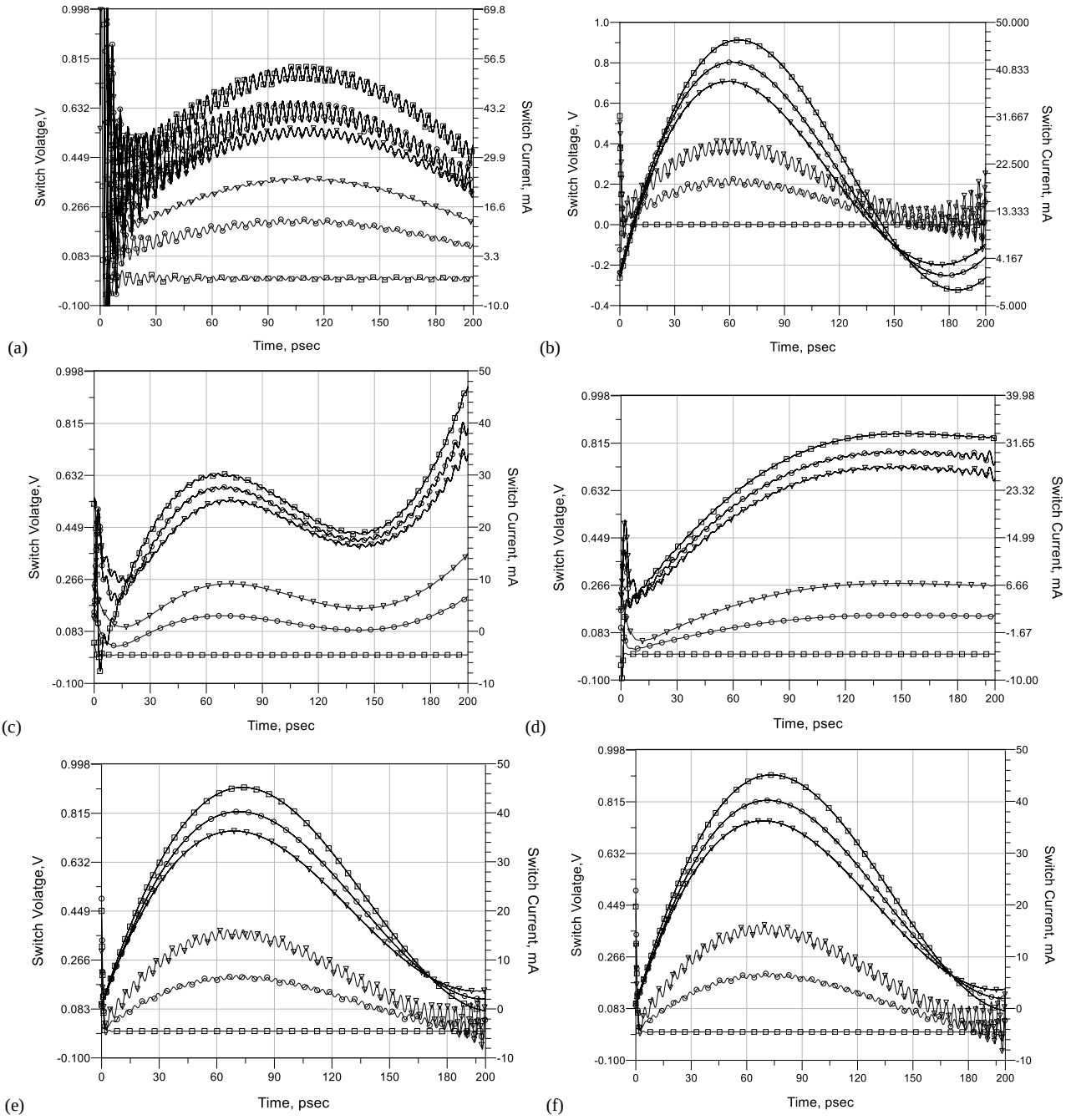

Figure 9. Switch Voltage (___) and Switch current (.....) at different values of R_{ON} for (a)T-I (b)T-II (c)T-III (d)T-IV (e) T-V (f) T-VI. ;-□- R_{ON}=0.01 Ω -○- R_{ON} =5 Ω -▽- R_{ON} =10 Ω

TABLE II. PEAK SWITCH VOLTAGE AT VARIOUS SWITCH ON RESISTANCES

R_{ON} (Ω)	Switch Voltage (Volts)					
	T-I	***T-II***	***T-III***	***T-IV***	***T-V***	***T-VI***
0.01	0.005266	0.000323	0.000452	0.000417	0.000516	0.000521
2.5	0.109182	0.121047	0.072018	0.078334	0.108042	0.107803
5	0.205274	0.226502	0.137867	0.148888	0.203764	0.203419
7.5	0.290791	0.317313	0.197324	0.213021	0.287116	0.286706
10	0.364634	0.396514	0.250232	0.271509	0.359973	0.359523

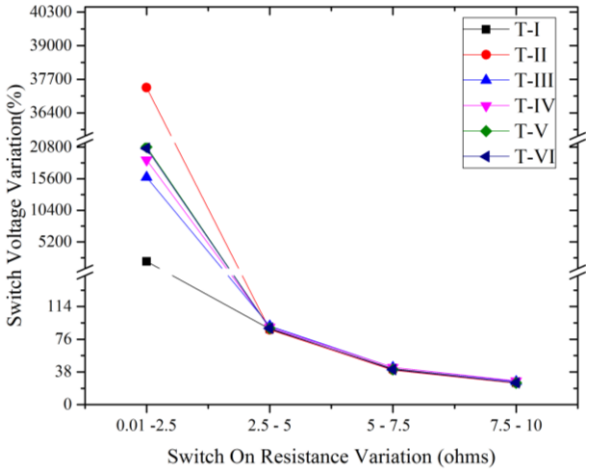

Figure 10. Switch voltage (%) as a function of R_{ON}

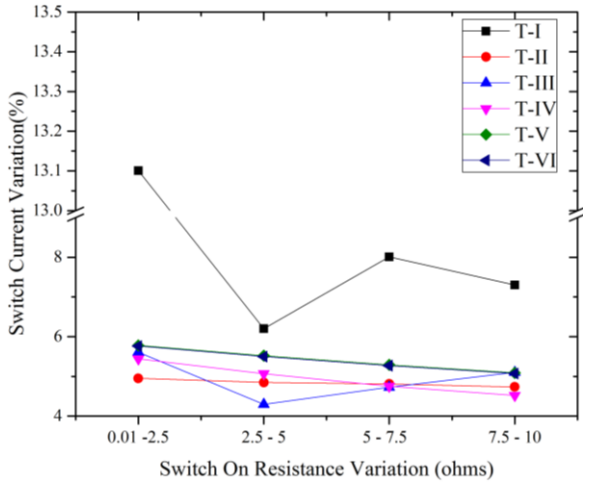

Figure 11. Switch current (%) versus R_{ON}

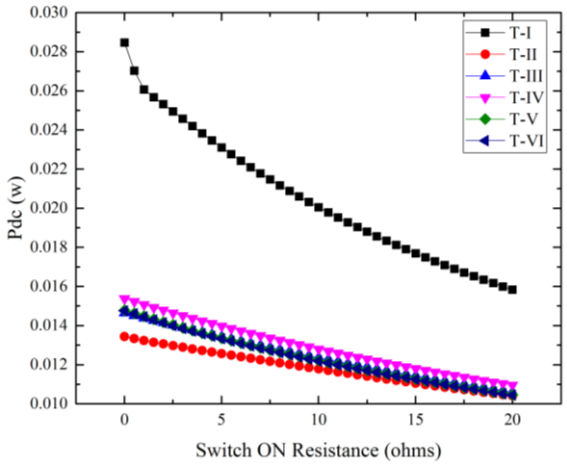

Figure 12. DC Power versus R_{ON} in various PA topologies.

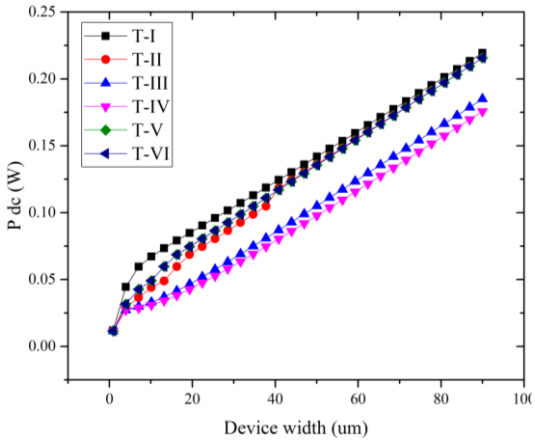

Figure 13. Total DC power consumed as a function of the width of the MOSFET

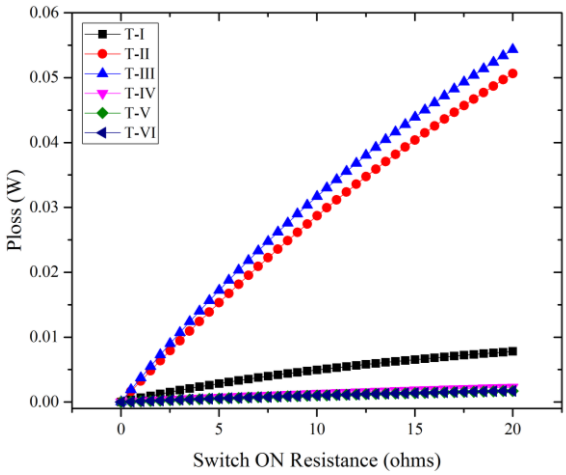

Figure 14. P_{loss} as a function of R_{ON}

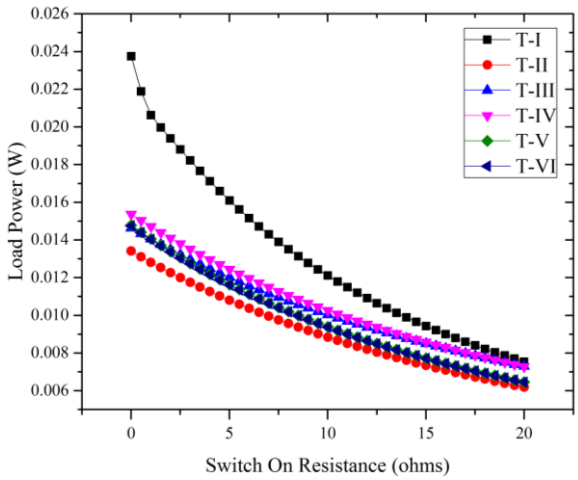

Figure 15. Total RMS load power as a function of R_{ON}

Where P_{dc} is the DC power supplied to the circuit and R_{load} is the load resistance. Fig. 12 shows the effect of R_{ON} on P_{dc} for all the topologies. As depicted in Fig. 12, the DC power decreases as R_{ON} increases. This is because of the decrease in supply current with the increase in the channel resistance. A similar effect is observed when all of the circuit topologies are realised using the MOSFET device from UMC. The ON-saturation resistance of a MOSFET is given by equation 10 [45].

TABLE III. PEAK SWITCH CURRENT AT VARIOUS SWITCH ON RESISTANCES

	Switch Current (mA)					
R_{ON} (Ω)	***T-I***	***T-II***	***T-III***	***T-IV***	***T-V***	***T-VI***
0.01	54.547	46.559	30.286	33.295	45.176	45.098
2.5	47.401	44.254	28.588	31.483	42.565	42.5
5	44.461	42.109	27.36	29.887	40.215	40.164
7.5	40.9	40.084	26.066	28.468	38.087	38.048
10	37.915	38.186	24.736	27.182	36.149	36.119

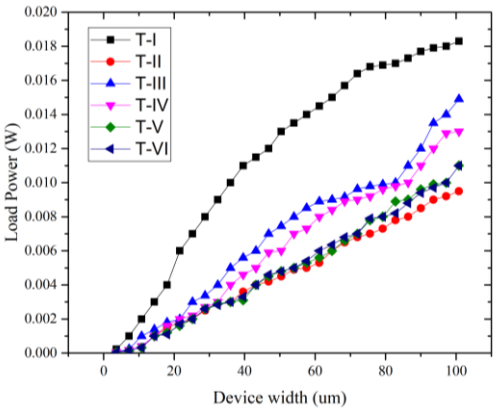

Figure 16. Total output power delivered to the load versus width of the MOSFET

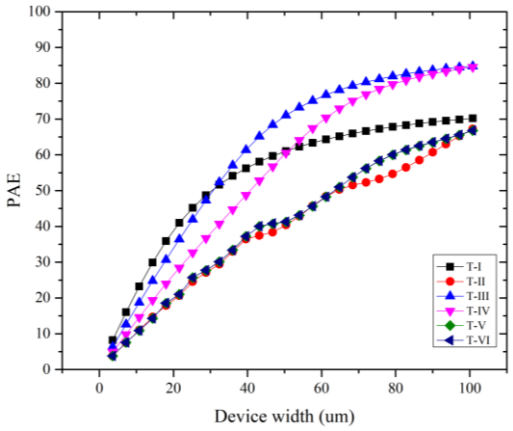

Figure 18. PAE versus width of the MOSFET

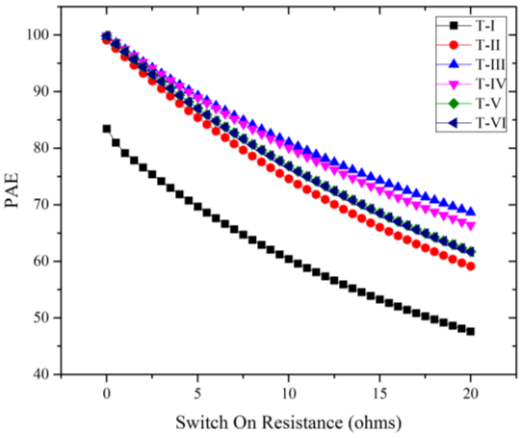

Figure 17. Power Added Efficiency (PAE) versus R_{ON} MOSFET

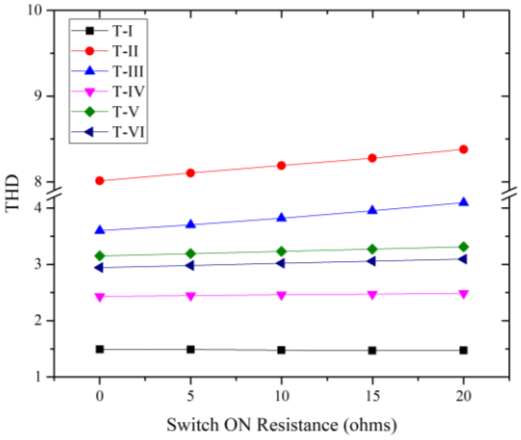

Figure 19. Total Harmonic Distortion versus R_{ON}

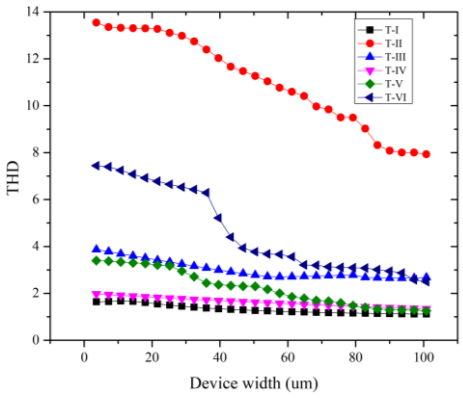

Figure 20. Total Harmonic Distortion at the load as a function of MOSFET width

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{w}{l}(V_{GS} - V_{th})} \quad (10)$$

Where the symbols have their usual meanings. As seen in equation 10, the MOS device's saturation resistance is the inverse function of the width (w) of the device. The variations of P_{dc} in the MOSFET are plotted against its width (µm) in Fig. 13. It is well evident that as the value of 'w' increases, P_{dc} also increases because of the decrease in RON. Moreover, this effect is more pronounced in T-I. The power loss as is given by equation 9 is illustrated in Fig. 14. As expected, the loss of power in the switch increases as the value of the switch ON resistance is increased.

Fig. 15 shows the dependence of load power (P_{load}) on the switch ON resistance. The output power delivered to the load drops as R_{ON} increases. This result exactly correlates with equation 9, since power loss will increase at greater values of R_{ON}. Similarly, the variation of load power for all the PA topologies realized using an RF MOS device versus its width is plotted in Fig. 16. It can be seen that, as the width of the device decreases, the power delivered to the load decreases as well, which is an expected result. Fig. 17 shows the variation of PAE as R_{ON} changes. With the increase in channel resistance, input power P_{in} decreases, since the equivalent DC resistance of the circuit increases. Thus, from equation 3, it is evident that the PAE drops with an increase in R_{ON}. Similar variation in PAE with respect to the device width is depicted in Fig. 18. As the device width increases, the ON resistance of the device decreases giving a boost to PAE. Total harmonic distortion for all the implemented class E topologies is plotted against R_{ON} and is presented in Fig. 19. As expected, THD drops with the decrease in saturation resistance since the harmonic content at the load increases. The corresponding values for the THD of the circuits realized using MOSFET as a switch is illustrated in Fig. 20. The figure clearly demonstrates the effect of non-linearity in the MOSFET. With the decrease in device width, R_{ON} increases, distorting the signal significantly, thus increasing THD.

6. CONCLUSION

The paper unveils various dependencies of power amplifier performance metrics due to the saturation resistance of the switching device. The results of this paper will assist PA design engineers to modify their design equations/circuit and make suitable trade-offs to enhance the performance for a particular application. In this paper, various class E PA topologies have been studied and critically analyzed for the effect of ON resistance of the switch on the PAE, output power and THD. Besides, power loss due to the finite value of R_{ON} has also been investigated. It has been observed that the switch ON resistance has a high dependence on the type of circuit topology. The PAE for the topologies designed with partially satisfying class E PA design equations is severely affected by variations at a lower resistance. The PAE and output load power is inversely proportional to the channel resistance while THD and power loss in the switch varies directly with it.

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